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# DIRECT INTERCONNECTION OF UNCASED ANALOG AND DIGITAL SILICON CHIPS INTO A BEAM--LEADED MATRIX

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## INTRODUCTION

A fabrication technique for direct interconnection of uncased integrated circuit chips in substantial arrays has been investigated. The technology consists of additive and subtractive chemical processes using fine-detail photo resist techniques for control of form factors. Considerable quantities of interconnections can be fashioned using a single piece of double-clad MYLAR laminate. The only physical terminations which need be made are to exit electrodes in the package enclosure and to the aluminum film electrodes on the planar surface of the integrated circuit chips. These connections are generally best accomplished using ultrasonics and face-up bonding.

## TECHNICAL ADVANTAGES

Some advantages of this type of hybrid microassembly are:

1. Each I.C. chip is mechanically and thermally anchored to a ceramic substrate by means of the large-area base of the chip. Superior environmental performance can be achieved compared to "flip-chip" hybrid arrays where the mechanical support and thermal flow is by means of metal bumps.

2. The quantity of man-made connections is reduced to the absolute minimum possible consistent with hybrid construction. This quantity of bonds is the same as found in flip-chip construction and is approximately one-half that of a comparable hybrid assembly using aluminum or gold jumper wires. The quantity of man-made bonds is approximately one-third that found in a comparable microassembly using individually cased chips.

3. Thin, ribbon-like beam leads are formed integral to the laminate part which provide a measure of mechanical flexibility during thermal expansion and contraction cycles. The ability to withstand thermal shock is judged intermediate, part way between the wire jumper construction and the flip-chip construction.

4. As in the wire jumper construction, visual inspection can be made of each individual bond and malfunctioning chips can be replaced at time of assembly.

5. Where the quantity of I.C. chips being interconnected in the hybrid array causes a considerable quantity of crossovers in the topology of conductor pathways, the separate beam-lead matrix part permits a density of hybrid chips which has not been reported for multi-levels of conductors deposited on a hybrid substrate.

6. In common with all other approaches to hybrid chip microassembly, a wide area of design freedom can be enjoyed by the engineer, since any mixture of uncased planar silicon chips available in the industry can be combined within a single microassembly array. This includes those chip devices which exhibit high impedance (F.E.T.), those which provide serial storage (M.O.S. shift registers), and those which offer high breakdown voltages, high cut-off frequencies, or high current-carrying capability.

## PRESENT LIMITATIONS

1. MYLAR is not fully satisfactory as the base for the interconnection layer since it exhibits complex shrinkage patterns at temperatures above 125°C. The resulting distortions can result in undesirable stresses on the beam leads. It is expected that KAPTON or other more stable material can be utilized to avoid this difficulty.

2. The methods used to register the chip lands to the finger patterns of the interconnection layer for this investigation were tedious and not satisfactory for production. Chip registration and handling devices are now available in the industry and should lead to resolution of this problem.

3. Interconnection yield needs to be improved if larger assemblies are to be made. Considerable difficulties were encountered with construction of the 42 chips article. Improved choice of materials for beam lead fingers and continued refinement of bonding schedules should provide improvements in yield.

4. Better means of matching the internal interconnections to external connections is needed. The test article on this contract required 151 external leads which was achieved by introduction of a secondary interconnection pattern resulting in unrealistic complexity of the complete assembly.

5. The techniques investigated covered only the interconnection of silicon chips. Fullest utility would include incorporation of other components and it is suggested that additional capability would be achieved by adding thick film components to the ceramic substrate and developing the techniques for extending the matrix interconnections to the thick film circuitry.

Suggestions for additional investigation and study are included as section II of this report.

## INTRODUCTION TO FINAL REPORT

This final report details the work performed on contract NAS-1-6023, "Direct Interconnection of Uncased Analog and Digital Silicon Chips Into a Beam Lead Matrix."

As defined in the statement of work, L-6496, the objective of this contract was to extend the microelectronic chip interconnection technology to the elimination of the flat pack and TO-5 container by directly connecting flexible printed circuit leads to the silicon integrated circuit die.

To obtain this objective, the work was broken down into tasks. This report describes these tasks in chronological event form and although there is considerable overlap and interlocking of events, an attempt has been made to place related items within the main task sections to which they were primarily related. These tasks are enumerated in detail in the Table of Contents so that specific items can be located rapidly.

The tasks, listed by section, are as follows:

| Section | Title |
|---|---|
| 1. | Materials Analysis. |
| 2. | Evaluation of Bonding Methods. |
| 3. | Resulting Characteristics from Chemofacture of laminates Using MYLAR. |
| 4. | Resulting Characteristics from Chemofacture of laminates Using KAPTON. |
| 5. | Physical and Chemical Compatibility. |
| 6. | Silicon Integrated Circuit Chip Technology. |
| 7. | Packaging Criteria for Test Vehicle. |
| 8. | Test Vehicle Requirements and Assembly. |
| 9. | Environmental Tests of Operating Items. |
| 10. | Engineering Documents. |
| 11. | Recommendations for Future Investigations. |

During the course of the program, a technical presentation based on this work was given at the 1967 Electronics Components Conference. This presentation can be found in the ECC 1967 Proceedings, entitled, "Direct Interconnection of Uncased Silicon Integrated Circuit Chips."

The conclusions from this work are as follows:

a. The ability of the test vehicles to withstand the environmental tests indicates that the principles of the beam leads is a sound one.

b. The fabrication difficulties experienced using MYLAR indicates that a dielectric material better able to withstand 175°C must be investigated.

c. The variables experienced when chemofacturing beam lead matrices would indicate that with the current state of processing, 42 I.C. chips are too many for a single assembly if one wishes to obtain high yield.

d. An overall electronic packaging scheme to enclose I.C. chip arrays is lacking and the makeshift substitutes caused considerable technical difficulties.

e. A method of simultaneously bonding the beam leads for an entire I.C. chip would be required for economic practicality.

A detailed review of the advantages and problems encountered with this technology is included in section 11. Suggestions are made for possible further investigation and development actions.

# 1.0 MATERIALS ANALYSIS

## 1.1 Metallization

By far the most universal practice in the IC industry is the use of aluminum on the silicon surface, but one company (Texas Instruments) is providing IC's with gold metallization. The widespread use of aluminum metallization on the chip in one respect limited the scope of our investigation since in our choice of bonding methods and plated riser laminates stressed the bonding to aluminized silicon chips.

In general, aluminum films about 1 micron (0.04 mil) in thickness are deposited on silicon to make IC interconnections. This thickness is designed to be thick enough to: provide good electrical conductivity of less than 0.01 ohms per square, withstand thermal alloying with silicon (ohmic drive-in), provide good adhesion and sufficient mass to accept lead attachment, provide abrasion resistance. On the other hand, the aluminization must be thin enough to: permit accurate etching and line definition, minimize thermal expansion differences relative to silicon and silicon dioxide.

## 1.2 Choice of Metal Foil

One of the criteria for a successful system is that it utilizes common, inexpensive materials readily available from several sources and where experience has been gained. The studies, then, did not consider any exotic, proprietary metals, nor expensive ones. It is felt all promising metals listed in common catalogs which could be formed into a laminate were included in our investigations.

## 1.3 Choice of Dielectric

The choice of laminate dielectric was narrowed down to one of two materials: Mylar (type A or T) or Kapton. Table 1.2 gives a comparative summary of their properties. Mylar has been very popular and much experience has been gained with it, whereas Kapton is a relatively new material which requires experimentation to determine if it is superior for the particular case in hand.

Electrical characteristics were of little concern. Major factors were: ease of selective etching, thermal expansion compared to the foil and the chip, and melting point.

For this project Mylar was selected for the test articles since its relatively low melting point would not be a deterrent when matrix operating temperatures are low. Mylar would be unacceptable if thermocompression bonding were used, but this is not the case. Kapton was being investigated primarily because of its greater dimension stability.

## 2.0 EVALUATION OF BONDING METHODS

### 2.1 Early Tests and Chip Items

Considerable effort was expended during the first quarter investigating the bonding of the interconnection on the "silicon die" to the beam leaded matrix. This effort was particularly concentrated on ultrasonic bonding of various metal foil fingers to aluminum land areas. Ultrasonics early showed signs of success. Other bonding methods tried were parallel-gap welding and pulse bonding. To simplify the studies, a particularly large chip from ITT Semiconductor Division was used having land areas of 10 x 10 mils.

Initial bonding studies were carried out by simulating the actual conditions. Specifically, narrow strips of foil were used to simulate the beam leads, and chips with completely aluminized surfaces were used to provide a much greater target area over the 10 mil square pads.

Throughout the studies, cleanliness was of utmost importance. Work pieces (chips, foil strips, sonotrode tip) were always cleaned thoroughly and then handled with tweezers and clean white gloves. Several literature sources claim ultrasonic bonding does not require greaseless surfaces, but no chance was taken. Later results proved the need for clean surfaces.

### 2.2 Ultrasonic Bonding

a. Set-Up - The initial ultrasonic bonding studies were carried out using a Sonobond Micropositioner, Model MP-20-L, equipped with a Model W-260-A Welding Head, and Model G-260-A Power Source. The chips were held firmly in place by cementing with Eastman 910 epoxy cement to a 2" square x 1/8" thick steel plate. This plate was then set over the Sonobonder's Vacuum Head for rigid mounting with reference to the sonotrode tip. This satisfies the requirement for firm mounting of the workpiece during ultrasonic bonding. The sonotrode tip angle was tried straight up and down and also $30^{o}$ from the vertical. Differences in results were negligible. Several sonotrode tip radii were tried, namely, 1/8" and 1/4", with neglible difference in results.

b. Metals Used - Many metals of varying thicknesses were attempted as listed in Table 2.1.

### 2.3 Pull Test Data

Measurements of pull in shear were made for ultrasonic bonding using a gram gauge designed for the purpose. A small loop was made using Eastman 910 cement on one end of the 1 mil foil strip used to simulate the beam lead. The other end was bonded to the chip pad. The tip of the gram gauge's arm was placed in this loop and force exerted until the bond broke or the gauge's maximum of 60 grams was reached. A successful bond was considered 5 grams or more. The three independent variables—power, time, and pressure—were varied one at a time to determine their effects.

### 2.4 Parallel-Gap Welding

a. Set-Up - The popular Hughes Model MCW550/VTA60 was used. Pulse amplitude and duration were varied independently. Values were initially set low and gradually increased. Distence between electrodes was decreased as much as practical

because electrode size already was large compared to chip pad size. Another variable, downward pressure of the weld head, was set to hold the finger firmly on the chip and was not varied.

b. Results - Several promising combinations were attempted but with no success. At lower energy levels, nothing occurred. Then at a certain point "burn-outs" in the metal fingers occurred suddenly. Further increases in energy levels also caused the pads to burn out.

TABLE 2.1

ULTRASONIC BONDING TO ALUMINUM PADS - FOILS ATTEMPTED - EARLY EXPERIMENTS

| Metal | Composition | Thickness | Successful Bond Yes | Successful Bond No |
|---|---|---|---|---|
| AL | Pure | 1 Mil | X | |
| CU | Pure | 1 Mil | | X |
| CU | Pure | 0.5 Mil | | X |
| NI | Pure | .7 Mil | | X |
| KOVAR | 54% FE, 29% NI, 17% CO | 1 Mil | | X |
| ADVANCE | 70% CU, 30% NI | 1 Mil | | X |

| Metal | Vacuum Deposition | Thickness of Base Metal | Successful Bond Yes | Successful Bond No |
|---|---|---|---|---|
| CU | AL | 1 Mil | | X |
| CU | AL | 0.5 Mil | Some Success | |
| CU | Nichrome - AL | 0.5 Mil | | X |
| KOVAR | AL | 1 Mil | | X |
| NI | AL | .7 Mil | | X |
| CU | AL | 1.5 Mils | | X |

| Metal | Plating | Thickness of Base Metal | Successful Bond Yes | Successful Bond No |
|---|---|---|---|---|
| CU | Tin - Lead | 0.5 Mil | | X |
| CU | Tin (Electroless) | 0.5 Mil | Possibly | |
| CU | Gold | 0.5 Mil | | X |
| NI | CU | .7 Mil | | X |
| NI | Tin - Lead | .7 Mil | | X |
| NI | Gold | .7 Mil | | X |
| NI | Gold (Electroless) | .7 Mil | Some Success | |

TABLE 2.2

RESULTS OF ULTRASONICALLY BONDING
1 MIL ALUMINUM FOIL TO ALUMINUM CHIP PADS

A. Power = 11, Clamping Force = 60 gms

| Sample No. | Time | Shear Test ($25^{o}C$) | Shear Test (After $150^{o}C$ for 20 Min.) |
|---|---|---|---|
| 1 | 20 (.92 secs) | > 60 gms | 53 gms |
| 2 | 19 (.83) | 55 | - |
| 3 | 18 (.74) | >60 | >60 |
| 4-10 | 17-5 (.66- .10) | >60 | >60 |
| 11 | 1 (.02) | 30 | - |

B. Time = 21 (1.02 secs), Clamping Force = 60 gms

| Sample No. | Power | Shear Test ($25^{o}C$) | Shear Test (After $150^{o}C$ for 20 Min.) |
|---|---|---|---|
| 16 | 9 | 43 gms | - |
| 12 | 20 | 60 | - |
| 13 | 30 | 60 | > 60 |
| 15 | 35 | 60 | >60 |
| 14 | 40 | 42 | - |

C. Time = 21 (1.02 secs), Power = 11

| Sample No. | Clamping Force | Shear Test ($25^{o}C$) | Shear Test (After $150^{o}C$ for 20 Min.) |
|---|---|---|---|
| 17 | 50 gms | 32 gms | - |
| 18 | 50 | 50 | - |
| 19 | 55 | >60 | 42 gms |
| 20 | 60 | >60 | 60 |
| 21 | >60 | >60 | 60 |

D. Time = 13 (.40 secs), Clamping Force = 60 gms

| Sample No. | Power | Shear Test ($25^{o}C$) | Shear Test (After $150^{o}C$ for 20 Min.) |
|---|---|---|---|
| 22 | 9 | 30 gms | - |
| 23 | 10 | >60 | >60 |
| 24-28 | 20-60 | >60 | >60 |

TABLE 2.2 (Cont)

RESULTS OF ULTRASONICALLY BONDING
1 MIL ALUMINUM FOIL TO ALUMINUM CHIP PADS

E. Time = 13 (.40 secs), Power = 11

| Sample No. | Clamping Force | Shear Test (25°C) | Shear Test (After 150°C for 20 Min.) |
|---|---|---|---|
| 29 | 50 gms | 50 gms | - |
| 30 | 55 | >60 | >60 gms |
| 31 | >60 | >60 | >60 |

2.5 Pulse-Bonding

a. Set-Up - A General Electric Square Pulse Bonder was used. Its set-up and operation was similar to the Hughes Parallel-Gap Welder (Section 2) with the addition of another variable, number of pulses. Settings were initially established at low values and gradually increased.

b. Results - Only a few of the more promising metal combinations were tried but with no success. One of the difficulties encountered was that the electrode tips readily clogged up with metal and required constant cleaning.

2.6 Vacuum Deposition of Aluminum to a Different Foil Metal

Early in the bonding studies an attempt was made to aluminize the underside of the finger to chips. This approach would permit the use of a metal with an easier etching cycle while at the same time provide a good aluminum-to-aluminum bond ultrasonically. In particular, ITT's several years' experience with copper could be utilized. Results did not show promise for this approach for chips having aluminum lands because the deposited aluminum did not adhere well to the base metal. When bonded ultrasonically, the deposited aluminum stuck to the chip land but tore away readily from the base metal.

2.7 Good Ultrasonic Bonds, Aluminum to Aluminum

Very strong aluminum to aluminum ultrasonic bonds were obtained that held up under considerable temperature stress. Bonds with higher than 60 grams shear force were regularly obtained in a wide range of settings. A wide range is most desirable in production runs. When working with fragile pieces, it is obvious that the smallest amount of energy possible should be used. Energy at the metal interface is proportional to all three variables. Roughly speaking, the product of power and time gives the energy available and clamping force determines how much of this energy is utilized at the interface.

2.8 Change to Copper Beam Leads

In the second quarter, a range of ultrasonic bonder parameter settings for energy level, clamping force, and time duration were located which are suitable for copper foil. Since the ultrasonic bonder could perform with the two most important metals being considered for the beam-lead matrix (aluminum and copper), most further bonding studies concentrated

on this method. This direction is consistent with present trends toward ultrasonic bonding being observed in the integrated circuit component industry.

## 2.9 Bonding to Narrow Fingers

Improvements in the chemofacture detail, reported elsewhere in Sections 3 and 4, permitted use of realistic finger patterns of beam leads instead of discrete strips of metal foil ribbon. As a result, detailed familiarity of practical requirements for successful bonds and methods of destructive testing to check the adequacy of the results was accomplished.

Several breakdowns were experienced in the operation of the ultrasonic bonder and as a result, considerable familiarity was obtained concerned with the transducer tool design, working tip resonances, etc. During the trouble shooting, it was discovered that the most minute contamination of the beam-leads or the silicon chip pad areas from human finger oils generally prevents successful bonding or at least requires unusually high energy levels and/or clamping force.

## 2.10 Bonding of Nickel-Plated Copper Beam Leads

The laminate suppliers were unable to deliver foils of 1/2 ounce soft rolled copper. The rolled copper provides ductility, while the thin gauge is necessary for good etching resolution of the 1.5 mil spaces often found between adjacent beam leads.

The use of electrodeposited copper foil in 1/2 ounce gauge led to quite fragile beam leads which easily cracked, probably because of the vertical copper crystal structure typical of most electrodeposited copper foils. An overplate of approximately 0.3 mils of "watts" nickel provided the extra strength and resistance to cracking.

The test vehicle utilized two widths of beam lead, 4 mils and 6 mils. These required somewhat different settings of ultrasonic bonding parameters. Typical results are shown in table 2-3. These readings were obtained on a Sonobond FC-160-H solid state supply, SN 125, using a 3 x 5 mil tip. The micropositioner was Sonobond Model M2016 with W260-A welding head. These settings were typical of those used to make the test vehicles.

TABLE 2.3

ULTRASONIC BONDING PARAMETERS, NICKEL/COPPER BEAMS

| | Narrow Beams | Wide Beams |
|---|---|---|
| Beam Lead Foil Thickness | | |
| a. Base Copper Foil | 0.70 mils | 0.70 mils |
| b. Nickel Overplate | 0.30 mils | 0.30 mils |
| Beam Lead Width | 4.0 mils | 6.0 mils |
| Silicon Pad Metallization | Aluminum | Aluminum |
| Power Reading | .25 (LO) | 1.25 (HI) |
| Delivered Power | .50 to .75 watt | .8 to 1.0 watt |

TABLE 2.3 (Cont)

ULTRASONIC BONDING PARAMETERS, NICKEL/COPPER BEAMS

| | Narrow Beams | Wide Beams |
|---|---|---|
| Time Duration Setting | 9 | 9 |
| Equivalent Time | 0.70 sec. | 0.70 sec. |
| Clamping Force | 100 grm | 100 grm |

2.11 Chip Die Bonding

a. Successful Method: At the present state of experience with the beam lead packaging approach, the best method of bonding chips to the alumina substrate is with silver filled epoxy. Other methods were considered but discarded. The silver epoxy used was TRA-DUCT 2902. Two things are critical, namely, applying just the right amount of silver epoxy on the alumina and applying it in the right spots. Trial and error using practice chips is the best method of determining the right amount. Desired is a thin layer of epoxy, roughly 0.1 to 0.3 mils, which covers most of the bottom surface area of each chip.

The procedure is a straightforward one but requiring a reasonably steady hand when done manually. A cleaned alumina substrate is set firmly into a specially made fixture. A mylar window pattern spacer is then set down over the substrate. A small drop of well mixed silver epoxy can then be placed through each of the windows onto the substrate. As each drop of epoxy is placed in the center of a window, it is spread out to a rectangular shape, slightly smaller than the window. This manual spreading out assures that most of the bottom of the chip is covered.

The chips are then placed through the windows onto the epoxy in proper order and positioned using Teflon-coated tweezers for handling. A beam lead matrix pattern is registered over the chips. With a clean dry, sharpened wooden stick, the first chip is pressed into the epoxy firmly and moved around slightly so its pads are lined up properly under the beam leads. This alignment is quite readily done. With care and the use of the soft wooden point, the chips aluminization pattern remains unmarred. All other chips are aligned similarly. If the right amount of epoxy is used, only the slightest amount will ooze out, readily fitting between the chip and mylar spacer. The chip array is then placed into an oven for curing the silver epoxy. The procedure (from applying the silver epoxy to aligning all 42 chips) took 50 minutes the first time that a pattern with 42 chips was tried. Since the silver epoxy has a pot life of 60 minutes and experience considerably shortens the registration time, this procedure appears to be satisfactory for the initial manual microassembly phases of up to about 50 chips in a single array.

b. Unsuccessful Methods: A similar cement was tried consisting of a formulation of epoxy filled with fine particles of alumina to provide superior thermal conduction. This was not successful because the alumina particles were as large as 1 mil, causing the microcircuit chip to seat at an unpredictable and elevated angle, interfering with good perpendicularity and clamping action in the ultrasonic bonding attachment, as well as posing the threat of potential shorts between the grounded edges of the chip and the beam leads.

Another unsuccessful method of die bonding was the use of Eastman 910, which is a cyano-acrylate monomer, but adhesion was too unpredictable with manual pressure-contact methods. Thermal conductivity between the heat generating I. C. chips and the alumina substrate is suspected to be quite poor, so this bonding scheme was not investigated any further.

## 2. 12 Durability of Die Bonds

A number of performance factors were investigated to determine the adequacy of bonding I. C. chips to an alumina substrate using silver epoxy cement. These were potential degradation of adhesion from high temperature soak and possible loss of die bonds through thermal shock cycles.

Arrays of chips were cured at +150°C for 1 hour. These subassemblies were left to soak at +175°C for several days. None of the chips could be dislodged using considerable sheer force. The subassemblies were then cycled from a stable +175°C into a $CO_2$ discharge and back into the +175°C oven. No degradation of the bonds could be detected.

The same die-bonded arrays were then subjected to long-term oven storage at various temperatures ranging between +125°C and +175°C for several months, interleaved with periodic room temperature examinations. No degradation of bond strength has been detected.

## 3.0 RESULTING CHARACTERISTICS FROM CHEMOFACTURE OF LAMINATES USING MYLAR

### 3.1 Preliminary Explorations

Copper and aluminum laminates having one-sided and two-sided foil coverings over MYLAR were used to form window openings and beam lead fingers which match the ITT Semiconductor Div. silicon chip SL300. These samples were used for realistic supplies of beam leads for the bonding experiments described in section 2, after the preliminary bonding experiments using ribbon leads were complete.

Surface etching experiments were conducted in both aluminum foil and copper foil to determine the etching resolution of conductor traces and fineness of finger patterns. Conductor densities in the range of 100 per inch (5 mil width and spacing) are easily etched in half mil foils.

### 3.2 Nuggets vs. Feedthroughs In Laminate Construction

Holes on 20 mil centers have been chemofactured in the foils and through the dielectric core. Metallic plating of nuggets in these holes showed some degree of shorting or bridging.

Experiments in selective deposition of a different metal over the laminate foil to serve as an intermediary or transitional metal on the beam lead fingers was conducted. Gold plating suitable for assisting in bonding to the gold lands found on certain vendors chip designs was easily performed.

Aluminum coating by vacuum deposition was performed on several laminates made from copper foil. Although the aluminum covers the irregular surface of the copper foil quite well visually, the adherence has not been adequate to pass pull tests after bonding to aluminum chip lands.

### 3.3 Plating on Aluminum (Gold/Copper/Nickel)

Gold, copper, and nickel were successfully electroplated on aluminum foil using the Alstan 70 process. This process is a proprietary process available from M & T Chemicals, Inc. consisting of an activating bath followed by a Bronze strike. Briefly the process is as follows:

1. Degrease the Aluminum part.
2. Mild Alkaline etch.
3. Water rinse.
4. Nitric or Nitric + Hydrofluoric acid dip.
5. Water rinse.
6. Activating Immersion (Alstan 75 solution)

7. Bronze strike

8. Water rinse.

The part is now ready for subsequent plating. The steps that follow will depend on the metal to be plated and the type of final finish required. It was found that normal procedures for electroplating the desired metal were effective after the aluminum had been treated with the above process. Thicknesses of the order of 0.001" were plated with excellent adhesion.

An attempt was made to selectively plate small pattern areas on Aluminum. This has not yet been successful because the photo-resists that have been tested to define the pattern have broken down in the Alstan solution.

The resists tested were KPR, Shipley AZ 340, and Dynachem 3140. An alternate approach which was successful was plating the entire aluminum piece with copper; etching the pattern in the copper; and then using the copper as a resist to etch the aluminum.

## 3.4 Etching Aluminum

An investigation was made to select the proper etchant of aluminum to achieve the definition needed to form beam leads to bond to the silicon chip. The following shows the solutions investigated and the results.

| Solution | Results |
|---|---|
| 20% Sodium Hydroxide | Etching too fast, to much undercut. |
| 10% Sodium Hydroxide | See above. |
| 10% Ammonium Hydroxide | No etching. |
| 10% Sodium Hydroxide +10 gas Ammonium Hydroxide | Etching accomplished but Definition poor |
| Ferric Chloride | Etching too violent. |
| 10% Cupric chloride | Excellent circuit pattern definition with .0065" lines. |
| 10% Cupric chloride +10% Hydrochloric Acid with Ultrasoncis | Adequate finger patterns etched. |

The best etchant thus far investigated is the cupric chloride-hydrochloric acid mixture used with ultrasonic energy. The ultrasonics is needed to remove the scale formed by the replacement reaction of Aluminum for Copper.

## 3.5 Factors Influencing Matrix Design

There are a number of chip design factors which influence the pattern details of the matrix:

a. The chip outside dimensions - in order to form window openings for jigging or registration.

b. The pad or land width - which determines the width of the beam leads or fingers.

c. The total quantity of pads or lands - which determines the perimeters of beam lead nuggets.

d. The chip thickness and tolerance on thickness - to determine overall build-up thickness of the matrix.

The economics of silicon integrated circuits require that the maximum possible number of chips be scribed from each master slice. Most digital chips were around 50 mils square at mid-1966 time frame. Analog chips run a bit larger, apparently because of extra space needed for critical resistors and capacitors required to establish the quiescent operating point.

The various window openings required to "tailor-fit" chips of these sizes or larger is easily performed.

The majority of fabricators use lands which range from 3.0 to 5.0 mils wide, round or square. Whether the device jumper leads are ball bonded or wedge bonded, one mil jumper wire is generally used with a spreadout of 2 to 3 in the bonding cycle. The industry-wide availability of fine 1 mil diameter gold and aluminum wire seems to have determined the practical minimum width of land, since the bonding machinery generally depends on operator eyesight to center the wire jumpers.

The most narrow beam fingers which can be expected is about two mils wide, to account for some mis-registration. This size is in keeping with the Bell Laboratories project for forming beam leads on special high speed-high voltage transistors. In that project, the beams are about 2 mils wide with about 8 mils of cantilevered overhang.

The use of laminated metal foils in the 0.1 to 1 mil range permits beam fingers to be etched directly to this 2 mil width, but the undercutting angles cause the cross-section to be trapezoidal. Should any of the bonding methods find this trapezoidal shape undesirable, the alternative method of building up the beam fingers by a plating process with subsequent chemical erosion of the laminate metal with selective etchants would be useful.

For maximum utility of both digital and analog chips, 14 lands per chip is rapidly becoming quite a popular number for lands on a single chip. To fit a ring of 14 rivet-like nuggets or feedthroughs around a window area which holds a chip requires a laminate area of 100 x 100 mils. Such an array of plated rivets can be standardized for any beam-lead configuration on chips up to about 60 x 60 mils, which accounts for most available chips. Special integrated circuit chips of larger die size would require custom artwork.

## 3.6 Requirements for the Matrix Laminate

There are a restrictive series of chemical and mechanical requirements for the double clad flexible laminate used as a beam land matrix. Some features which would enhance the yield or quality of the matrix as a higher density network of conductors would not be favorable when considering reliable bonding of the beam lead fingers to the chip lands. Further factors which would provide good metal etching and plating characteristics would not be suitable for chemofacture of the dielectric core. Among these factors examined in order to properly specify the laminate were:

a. Chemical purity and alloy content of the metal foil.

b. Hardness and temper of the metal.

c. Surface chemical treatment and mechanical roughness to assist in adequate adhesion to the dielectric.

d. Type of adhesive, its temperature rating, and resistance to industrial solvents and cleaning fluids as well as the dielectric digestion cycle.

e. Foil uniformity of thickness and overall smoothness of laminate.

f. Ductility and temperature coefficient of expansion.

g. Freedom of scratches, dents, or other blemishes which could be the site of "crack propagation" types of failure.

h. Capability for surface plating of specific metals which might be required as intermediaries or to form feed through nuggets or rivets by chemofacture.

## 3.7 Chemofacture Cycle

Although certain steps may be out of sequence or combined into a single step, the following sequence of activity is representative of the methods used to fabricate the beam-leaded matrix of the initial single layer design:

a. Chemically cut out holes for all beam-lead rivets and outside world nuggets using single or double sided hole cutting artwork.

b. Mask surface metal and plate rivets and nuggets in the specified metal.

c. Chemically cut out window openings for all chip locations using single sided artwork for windows.

d. Resist under-side of top foil in each window area by metallic or photoresist methods.

e. Register surface artworks for electronic interconnection and finger patterns to both photosensitized surfaces of laminate simultaneously using rivets as registration features.

f. Fine detailed etch and surface condition the upper and lower foils to form the completed matrix.

## 3.8 Plated Nickel Fingers

A method was devised for making a standard copper matrix having nickel fingers. It consisted of first plating a nickel pattern of fingers on the copper. This plating later acted as a resist so the copper surrounding the fingers was etched away. Then after the windows were etched from the underside, the copper under the nickel plate was removed, leaving nickel fingers. The quality of the fingers was only fair, but the experiment demonstrated how, with selective plating and etching, various metal combinations can be achieved.

## 3.9 Types of Laminate Investigated

During the second quarter the emphasis in the chemofacture area was placed on experiments which would determine the proper materials and processing necessary to fabricate mechanical models of the anticipated final test vehicle. Also samples were fabricated for further bonding studies.

The following laminates were investigated as possible material for the final circuit:

(a) Copper Laminate
One oz. electrodeposited copper on one mil MYLAR with polyester adhesive.

(b) Copper Laminate
One oz. rolled copper on one mil prestressed MYLAR with polyester adhesive.

(c) Copper Laminate
One oz. electrodeposited copper on one mil KAPTON with Teflon adhesive.

(d) Aluminum Laminate
One oz. aluminum on one mil MYLAR with polyester adhesive.

(e) Aluminum Laminate
One oz. aluminum on one mil KAPTON with Teflon adhesive.

(f) Aluminum Laminate
One-half oz. aluminum on two mils MYLAR with polyester adhesive.

## 3.10 Copper Clad Laminate Chemofacture Processes

The choice of copper laminate for further fabrication was (b) above because the rolled copper is better able to withstand thermal excursions and the prestressed MYLAR will digest slightly faster than the raw MYLAR, i.e., 45 seconds digestion of the window pattern in prestressed MYLAR as opposed to one minute digestion for the same pattern in the other. A basic list of process steps for copper foil on MYLAR are as shown in Table 3.1 and Table 3.2. (These basic steps were modified for final article fabrication).

TABLE 3.1

PROCESS STEPS - STANDARD RIVET PATTERN IN COPPER/ MYLAR LAMINATE

1. Photo Resist Dot Pattern
2. Etch Copper Holes
3. Remove Photo-Resist
4. Digest Dielectric
5. Plated Through-Hole Process
6. Photo-Resist Rivet Pattern
7. Electroplate Rivets
8. Remove Photo-Resist

TABLE 3.2

PROCESS STEPS - CUSTOM FEATURES IN COPPER/MYLAR LAMINATE

1. Photo Resist Process for Window Pattern
2. Etch Windows in Foil
3. Remove Photo-Resist
4. Digest MYLAR Dielectric
5. Photo-Resist Process for Surface Matrix Pattern
6. Etch Conductor and Beam Lead Pattern
7. Remove Photo-Resist
8. Final Inspection

## 3.11 Aluminum Clad Laminate

The only aluminum laminate which gave fairly satisfactory results was the one oz. aluminum on MYLAR (d) above. A minimum of one oz. of aluminum is necessary due to the chemical erosion that takes place during the processing. The state-of-the-art for fabricating aluminum matrices has not yet reached the sophistication of copper matrices. The main problems in this area were the more severe undercutting of aluminum during etching and finding a suitable, easy to use, etch resist. The best etch resist was to overplate with copper, then use the copper as the resist for aluminum.

The series of process steps used is shown in Table 3.3 and Table 3.4.

TABLE 3.3

PROCESS STEPS-STANDARD RIVET PATTERN IN ALUMINUM/ MYLAR LAMINATE

1. Degrease Aluminum Surfaces
2. "Alstan 70" Process
3. Copper Plate
4. Photo-Resist Process for Dot Pattern
5. Etch Copper
6. Etch Aluminum
7. Remove Photo Resist
8. Digest MYLAR
9. "Alstan 70" Process
10. Copper Plate
11. Plated Through-Hole Process
12. Photo Resist Rivet Pattern
13. Electroplate Rivets
14. Remove Photo-Resist

TABLE 3.4

PROCESS STEPS-CUSTOM FEATURES IN ALUMINUM/MYLAR LAMINATE

1. Photo-Resist Process for Window Pattern
2. Etch Windows Through Copper
3. Etch Windows Through Aluminum
4. Remove Photo Resist
5. Digest MYLAR Dielectric
6. "Alstan 70" Process
7. Copper Plate
8. Photo-Resist Process for Surface Matrix Pattern
9. Etch Conductor and Beam Lead Pattern
10. Final Inspection

## 3.12 Finalized Methods of Forming Beam Leads

The artworks shown in Fig. 8-3 to Fig. 8-13 were developed during the third period. In order to obtain statistically significant data, six transparent pairs of each artwork set were used. A set of six laminates could be processed at one time, permitting more efficient use of technician time and showing up the variations experienced in the different process steps.

Approximately 60 beam lead matrices were chemofactured as well as about 30 exit layers and 20 dielectric spacers. Various alterations in artwork factors were used as well as alterations in the sequence of processing steps and alterations in the detailed procedures used in some of the processing steps.

Two primary methods of forming the beam leads were used, one resulting in solid nickel beam leads, the other resulting in nickel beams having original copper foil as an underlayment. The yield of high quality beam lead matrices was higher for the process resulting in solid nickel beams, but plating bath maintenance was difficult, resulting in lack of consistency in the deformation and ductility properties of the beams. The alternative process required a manual touchup step which was less than perfect in results, causing a small percentage of lost beam leads and consequently resulting in use of the blemished matrix for experiments only.

## 3.13 Cutting Holes in Mylar

The technique used to form holes in the MYLAR requires the use of metal foil as a pattern mask, since the concentrated acid also rapidly attacks any of the organic photosensitive resists tried so far. Ultrasonic energy is used to transport the disintegrated MYLAR away from the openings in the metal foil thus permitting further attack of the MYLAR.

If the etched holes in the metal foil are in the range of 0.5 mil to about 20 mils, rapid and well controlled cutting takes place simultaneously from both sides of the laminate, resulting in consistently clean openings through the material. Above 20 mils, however, a nodal pattern of attack begins where cut-through spots occur at the usual timing, while areas in between take two to three times longer to digest completely through the dielectric. When the timing is increased by such factors in order to digest the stubborn areas, there is a serious undercutting of the MYLAR at the nodal points where cut-through was achieved quickly. The result is a characteristic "wavyness" to the edge of the MYLAR hole. Present theory presumes that the effect is caused by standing waves in the metal foil which are pattern sensitive to the ultrasonic frequency being used.

Since the effect does no harm to the feed-through eyelets, it is not considered serious. The "waviness" around the edges of the chip access windows did interfere with the ragged silicon chip side walls, however, and required enlargement of all window artwork patterns.

## 3.14 Revised Process Step Order

Table 3.1 and Table 3.2 above are representative of the basic process steps. However, the conductor line widths and the width of the beam leads were about 10 mils. The requirement to use currently available chips has necessitated development of beam lead fingers as narrow as 3 miles, since this is the bonding pad minimum limit usually found on I.C. chip aluminization.

It was quickly discovered that satisfactory results could not be achieved with the artwork shown in Figure 8-4. Experiments showed that the nickel electroplating of the feed-throughs had to allow a surface buildup of about 0.5 mil minimum for reliable feed-through performance. This buildup of nickel above the laminate surface prevented the beam lead transparency from establishing emulsion to emulsion contact and resulted in severe shadowing and reduction in the 4 mil beam lead width. By plating the surface beam leads prior to nickel buildup in the feed-through holes, the problem was solved. The tables should, therefore, be revised as follows:

TABLE 3.1 (Revised)

PROCESS STEPS - FORMING CUSTOM FEED-THROUGHS IN COPPER/MYLAR LAMINATE

1. Photo-Resist Dot Pattern
2. Etch Copper Holes
3. Remove Photo-Resist
4. Digest Dielectric
5. Plated Through-Hole Sensitizing
6. Photo-Resist Surface Beam Leads and Conductors
7. Plate Thin Nickel Pattern on Surface and In Holes
8. Strip Photo-Resist
9. Photo-Resist Resist Pattern
10. Electroplate for Rivet Buildup
11. Remove Photo-Resist

TABLE 3.2 (Revised)

PROCESS STEPS - FORMING LARGE CUTS AND FINISHING MATRIX

1. Photo-Resist Window and Tool Pattern
2. Etch Windows in Foils
3. Remove Photo-Resist
4. Digest MYLAR Dielectric
5. Etch Away All Copper Not Covered by Nickel
6. Final Inspection

In working with the fine detail artworks, the one ounce copper foils were too thick to provide the necessary small clearances of 2 mils. Almost all successful matrices and exit layers have been fabricated with one-half ounce electrodeposited copper foils on a one mil preshrunk MYLAR core. The thinner foil provides correspondingly less undercutting and permits high yield without residual copper metal bridging at two mil spacing. The above process steps use this thinner foil laminate.

### 3.15 Plating Border

Intolerable variations in pattern plating were experienced on the original artwork transparencies. Severe buildup of metal would occur at pin holes or sparsely located conductors or lands. In pattern areas of high conductor concentration, a serious deficiency of plating buildup was experienced.

The traditional plating thieves proved to be ineffective in providing an even field of plating current density for the very fine detail patterns. A plating border had to be added around the periphery as shown in Figures 8-4 and 8-6. Adjusting the gross area of the thieving border and the effective distance of the border from the center of the matrix was required to provide an even buildup of electroplated metal over the entire matrix regardless of local variations in the pattern.

### 3.16 Registration Accuracy

The laboratory scheme used to register transparencies to each other and to the in-process laminate was quite crude, consisting of double sided pressure-sensitive tape, an eye loop of low magnification, and considerable patience on the part of the technician. In use, each matched set of flexible transparencies tended to go out of registration by about one mil. With manual registration of the transparencies to the in-process matrix, as much as 2 mils of registration error results due to the tedious registration sequence along the diagonal span of two inches. These manual processes for critical registration result in a matrix reject rate of about 30 percent.

Inquiry was made to several manufacturers of split optics alignment apparatus as used in the silicon I.C. wafer artwork registration activities at semi-conductor houses. It appears that low cost investment in a modified machine would virtually eliminate these registration errors. The proposed scheme would entail use of the split optics to register one transparency to the other, then precise mechanical translation of one transparency out of the way while the laminate is registered. Finally, the second transparency would be returned, depending on mechanical precision to assure congruency of all three patterns while the double sided ultraviolet light exposure takes place.

### 3.17 Feed-Through Endurance Tests

A method had to be devised to check the statistics of the plated through holes. Since each beam lead matrix part has over 700 feed-through holes in it with a clearance diameter of less than 5 mils, it would be impractical to visually inspect all of them. Microsections of "typical" feed-through holes were made to establish sturdy looking proportions to the plating, but the cross sections are costly to prepare and, therefore, could not be relied on for statistical inference as to the constancy of the feed-through plating quality.

Continuity test patterns were chemofactured which used a form of "weaving" pattern which passed back and forth through 166 feed-through holes. A quantity of 18 test matrices were processed through the established chemofacture steps.

The test matrices were electrically put in series and a current of 400 milliamperes passed through the entire quantity of 2988 feed-throughs.

There were no initial failures; and, after 5500 hours of operation in an unprotected but closely confined sandwich of stacked up test laminates in a room temperature environment, no indication of change in resistance or signs of corrosion could be detected. At the conclusion of the test, there were more than 16 million nugget hours of operation at 5°C above room ambient without any failure.

### 3.18 Constancy of Physical Properties of Plated Beam Leads

Trustworthy performance of the beam leads depends heavily on the physical properties of the pattern-plated beam leads. Any thickness variation must be kept within close limits so that the ultrasonic bonding remains constant. Contaminates of an organic nature in the plating bath quickly change the crystal growth patterns and hence drastically alter the ductility and bending resistance of the beam leads.

### 3.19 Matrix Yields and Maintenance of Baths

The ability to chemofacture complex high density beam lead matrix laminates has been demonstrated using several alternative approaches. Using rather basic apparatus and procedures and very little help from alignment apparatus or well controlled chemical processes, a final yield of better than 25 percent can generally be achieved.

Addition of alignment mechanisms and some feedback control in the chemistry should result in a rather high yield of good quality matrices. Such action was not taken on this contract, however, since the quality of the accepted chemofactured products was sufficient to demonstrate the goals set up in the work statement.

When a freshly made nickel bath has been stabilized, the resulting nickel beams exhibit a reliable amount of plastic deformation in the bonding cycle, forming very strong ultrasonic bonds. These beam leads also can be bent back and forth through a 90 degree arc and at least thirty cycles before cracking.

As the nickel bath ages, the inadequate maintenance causes the resulting beam leads to become quite stiff and springy with very little plastic deformation from the ultrasonic tool tip and often cracking with as few as three or four bend cycles. The lack of consistently strong bonds and the fear of failure in vibration because of the brittle condition caused a temporary halt to the use of all nickel beams.

Of the alternate plating methods available to us- gold and copper, we chose copper as a "backup" method to sustain the activity in fruitful directions because of the favorable metal interface between aluminum and copper. A thin veneer of nickel is used over the copper to provide tensile strength to the beam leads, but the copper is used at the interface to the aluminum I.C. chip lands to assure a favorable ultrasonic bond condition.

## 4.0 RESULTING CHARACTERISTICS FROM CHEMOFACTURE OF LAMINATES USING KAPTON

### 4.1 Suitable Laminate Materials

An investigation was made to determine the feasibility of using a laminate material with KAPTON as the dielectric instead of MYLAR. The main advantage of KAPTON over MYLAR is that it would allow the test vehicle to withstand a wider temperature range than is possible with MYLAR. It was found that a satisfactory beam-lead matrix could be fabricated with copper-KAPTON combination. As yet, it is not possible to fabricate an aluminum-KAPTON combination because the chemicals used to digest the KAPTON are extremely corrosive to the aluminum. The chemicals used for digestion were either sodium hydroxide or concentrated sulfuric acid. Both of these will attack aluminum readily.

Although both chemicals will digest the KAPTON, the sulfuric acid is preferred as it gives a clearer definition of the dielectric holes. The hydroxide solution will digest somewhat faster but the edges of the KAPTON are more ragged. If KAPTON is to be used as a dielectric in a laminate matrix, adjustments will have to be made in the artworks to compensate for the undercutting of the KAPTON. For example, when digesting KAPTON through a five mil diameter hole in the copper, the resulting hole cut by digestion in the KAPTON was approximately ten mils in diameter. Part of this problem is due to the Teflon adhesive which is commonly used to bond the copper to the KAPTON. The solutions used to digest the KAPTON attack the Teflon adhesives more rapidly than the KAPTON.

## 5.0 PHYSICAL AND CHEMICAL COMPATIBILITY

### 5.1 Full Tests on Bonded Beam Leads

The physical and chemical compatibility of the materials used to form an assembly of uncased silicon chips can be established with confidence only by means of a realistic simulation or actual construction of the proposed assembly. At the present state of progress, there has been evaluation only of the beam leads to the chip lands without repeated or sustained stress of any kind except an artificial pull test with a mechanical gram gauge and an associated heat soaking as previously described.

As described in Section 2, any beam lead bond which would not withstand a shear test of five grams was considered unacceptable. A nominal "design center" of 25 grams was tentatively established for this shear test since a beam lead of aluminum having a cross section of 8 x 1 mil tends to pull apart at about 80 to 100 grams, depending on the temper or ductility of the metal. This level of pull is considered very high compared to the shear pulls to be expected in a realistic assembly. It is a convenient measure, however, of comparative results, and it provides a good safety measure for aging effects and the typical departures from ideal assembly conditions which is to be expected.

### 5.2 Proposed Assembly of Matrix to Chips

The assembly, for purposes of this compatibility study, consists of five basic parts:

1. The integrated circuit chips,
2. The chemofactured beam-leaded matrix,
3. The insulating or supporting medium,
4. The mechanical and thermal support, and
5. The overall package and connector structure.

These parts are analyzed in the following paragraphs for considerations of compatibility of materials.

### 5.3 Uncased Chip Physical Requirements

These chips are presently available with vacuum-deposited lands in aluminum and, to a lesser extent, in gold. There are laboratory attempts in various parts of the device industry to alter the pad or land surface for some assembly advantage, such as the IBM "flip-chip", but such developments are outside the scope of this contract.

The edges of chips are generally scribed and cracked apart. This method of separating the silicon slice into chips tends to form slanting surfaces on two or more edges of the chip due to the nature of the crystal orientation.

Another method of dicing the silicon slice into chips is some form of liquid "homing" or "sawing" on a minute scale similar to the cutting done in a marble or granite quarry. This approach wastes more slice surface in that the kerf allowance is larger, but some manufacturers feel that this loss is counteracted in a higher yield of mechanically sound chips. Although chips of this refined edge characteristic ideally fit the locational concept of "window" openings, at this time the better quality of edge definition is not considered a requirement to prevent incompatibilities.

The normal Quality Control features for silicon chip fabrication and handling could have serious effects on the integrity of the assembly. Such blemishes as faulty metallization, inadequate adhesion of the metal land areas, contaminated chip surface, corroded lands or conductors, scratches, etc., can all be causes of assembly failure if not screened out by the Quality Control procedures.

## 5.4 Dimensional Stability of the Beam Lead Matrix

The dimensional stability of the Mylar and copper foil laminate depends on three factors: total normal coefficient of thermal expansion in the Mylar and its adhesive, the normal coefficient of thermal expansion in the copper and plated-on metal, and the residual stresses placed in the mylar film. The latter factor causes "free standing" Mylar to shrink on its first exposure to elevated temperatures. Kapton behaves in the same way but the temperature required for a given shrinkage is much higher.

Once exposed properly, the dielectric film thereafter exhibits the normal thermal coefficient of expansion, provided that the exposure temperature used to pre-shrink the material is not closely approached. Since one requirement for the test vehicle is that it withstand +125°C continuously and thermal shock to +175°C, all laminates were preshrunk after the chemofacture processes were complete but prior to registration with the array of I.C. chips.

A number of beam lead matrices and exit layers which were rejected due to plating or etching imperfections were carefully preshrunk to determine the shrink factor. The following procedure was used.

1. Oven pre-heated to between +175 and +180°C
2. Each specimen sandwiched between glass slides and weighted down with a one pound weight.
3. One hour, two hours and 24 hours oven exposure were used.
4. A precision photo-transparency was then corner registered to each cooled specimen and the differentials caused by shrinkage measured on a comparitor microscope.

All specimens were chemofactured from a 1 mil Mylar and the reduction in an original 1.100 inch span was measured. The plating border was cut off prior to shrinking because preliminary tests showed that this metal border was strong enough to prevent shrinking and defeated the intent of the procedure. The results are quite dependent on how much surface metal has been left on either or both surfaces in the direction of measurement. Measuring across an open area shows the most shrinkage, while measuring along the direction of a lengthy conductor shows the least shrinkage:

TABLE 5.1

SUMMARY OF MATRIX SHRINKAGE MEASUREMENTS

| | 1 Hour | 2 Hours | 24 Hours |
|---|---|---|---|
| a. No longitudinal conductors | 1.80% | 2.10% | 2.15% |
| b. Longitudinal conductors (one side) | 0.90% | 1.10% | 1.12% |
| c. Longitudinal conductors (both sides) | 0.60% | 0.70% | 0.71% |

As a result of this amount of shrinkage, exit tabs completely miss the test board pc lands at one end if registered at the other end of one row of tabs. Since glass restraining plates are used, the metal conductors are forced to take a "roller-coaster" type of wrinkle with a peak-to-peak excursion limited to the height of the nickel exit nuggets, which is about 5 mils. If the quantity of longitudinal conductors in the direction of measurement is low, then the shrinkage is high, causing more hills and valleys along the conductors. If the quantity of longitudinal conductors along the direction of measurement is high, the shrinkage is much less and the number of physical kinks which the conductors must take are correspondingly fewer.

## 6.0 SILICON INTEGRATED CIRCUIT CHIP TECHNOLOGY

### 6.1 Results of I.C Vendor Survey

Since our interconnection studies depend so heavily on present silicon integrated circuit technology, we conducted a survey in the spring of 1966 on some major silicon integrated circuit manufacturers in order to determine die and land sizes as well as metallization processes presently in use and/or under development.

The following manufacturers were contacted:

Fairchild
Motorola
Sylvania
Texas Instruments
Westinghouse

Replies were received from all except Motorola. Answers are summarized below:

A. Chip Sizes

Fairchild

| | | |
|---|---|---|
| Digital | DTL 945 (FF) | 40 x 40 mils |
| | DTL 930, 962, etc | 37.5 x 37.5 mils |
| Linear | 710 | 35 x 35 mils |
| | 702A | 45 x 45 mils |
| | 709 | 50 x 50 mils |

Sylvania

| | | |
|---|---|---|
| Digital | Gates | |
| | SG4, SG24 | 49 x 32 mils |
| | SG5, SG6, SG10 SG11 | |
| | SG12, SG15, SG17, SG18 | 45 x 35 mils |
| | SG21, SG23, SG25, SG26 | |
| | SG27 | |
| | SG7, SG9 | 46 x 40 mils |
| | SG8, SG28, SG29 | 64 x 41 mils |
| | SG13, SG16 | 80 x 32 mils |
| | SG14, SG19, SG22 | 55 x 50 mils |

Texas Instrument

| | |
|---|---|
| Minimum size | 5 x 35 mils |
| Maximum size | 65 x 165 mils |

Westinghouse

| | |
|---|---|
| Digital | 42 x 45 mils |
| | 41 x 84 mils |
| Linear | 50 x 50 mils |
| | 60 x 60 mils |

B. Land Dimensions and Spacings

Fairchild

| | |
|---|---|
| Minimum diameter | 4 mils |
| Minimum spacing | 0.5 mil |

Sylvania

| | |
|---|---|
| Average dimensions | 3 x 5 mils |
| Spacing patterns | optional 0.5 mil |

Texas Instruments

| | |
|---|---|
| Dimensions min. | 3 x 3 mils |
| Dimensions max. | 5 x 5 mils |
| Spacing between leads | 0.5 mil |
| Spacing between land and lead | 2 mils |
| Spacing between lands | 3 mils |

Westinghouse

No reply to this item.

C. Metallization Available

Fairchild - Aluminum metallization; aluminum wire

Sylvania - Aluminum metallization; aluminum wire

Texas Instruments - Aluminum metallization; gold wire, gold metallization; gold wire

Westinghouse - Aluminum metallization; aluminum wire, Aluminum metallization; gold wire

D. Price and Availability of Chips

Fairchild - Wafers can only be sold to licensees. Other customers can, however, purchase individual chips. Chips are sorted at 25°C. Pricing is negotiable, based on specifications and quantity considerations.

Sylvania - The price of chips is one-half the Industrial Standard price of any contract for the equivalent circuit. Units can be delivered within 2 - 3 weeks ARO. All chips are 100% d.c. - probed.

Texas Instruments - TI indicates: "it would be extremely difficult to supply dice in quantities of less than several hundred of any given type. Dice probe is 60 - 70 percent of finished device price, availability is 4 - 6 weeks."

Westinghouse - Westinghouse is not actively marketing chips at this time. They do offer the Westinghouse WS-177-Insta Circuit, a monolithic "master slice" dice mounted in an unlidded flat pack or 10-pin TO-5 header. This unit is intended for IC breadboarding applications.

E. Testing, Shipping, Handling of Chips

Fairchild

All units are tested in wafer-form. Dice are shipped in wax, although work is being directed toward development of a method of shipping dice on plastic die plates. The same care must be exercised in handling IC chips as in handling normal transistor chips.

Sylvania

Sylvania suggests that the customer rely on 100% d.c.-probe testing. Sylvania chips are packed and shipped in plastic nesting pallets. Sylvania's experience is that minimum handling is the best method of preserving chip physical and electrical integrity.

Texas Instruments

IC's are tested in wafer form at room temperature for a selected number of d.c. tests and then shipped after scribing into bars. Transporting and shipping of chips is a problem not yet satisfactorily resolved. Paraffin and other materials have been used.

## 6.2 Analysis of Chips Used in the Test Vehicle (Final Plan)

With the definitization of the logic diagram, ITTFL print 2309494, to issue B (Figure 8-1) the following chip complement was required:

TABLE 6.1

LIST OF CHIPS USED IN TEST VEHICLE

| Chip Qty. | Signetics Type | Size W x L (Mils) | Used Pads | Total Bonds | Operating Chip Power | Operating Dissipation |
|---|---|---|---|---|---|---|
| 8 | SE 124-C RST Binary | (66 x 57) | 10 | 80 | 25 mw | 200 mw |
| 8 | SE 155-C Line Driver | (48 x 47) | 10 | 80 | 15 @ 9.3 mw<br>1 @ 5.8 mw | 198 mw |
| 1 | CS 732-C Input Expander | (42 x 48) | 14 | 14 | 1.5 mw | 1.5 mw |
| 8 | SE 106-C Diode Array | (42 x 48) | 10 | 80 | 15 @ 0 mw<br>1 @ 1.5 mw | 1.5 mw |
| 8 | SE 116-C Dual Gate | (57 x 47) | 14 | 112 | 15 @ 9.3 mw<br>1 @ 12 mw | 152 mw |
| 8 | CS 730-C Dual Gate | (57 x 47) | 14 | 112 | 15 @ 9.3 mw<br>1 @ 12 mw | 152 mw |
| 1 | SE 156 Line Driver | (48 x 47) | 8 | 8 | 1 @ 34 mw<br>1 @ 9.3 mw | 44 mw |
| 42 | I.C. Chips | 4 Sizes | | 486 Total Used Beam Leads (170 ma @ +4.4 V) | | 749 mw |

## 6.3 Receipt of NASA Furnished Chips

On 3 April 1967, the following quantities of Signetics I.C. chips were received on glass plates with paraffin was sealing:

| Plate | Type | Qty. |
|---|---|---|
| #1 | CS 732-C | 5 |
| #2 | CS 730-C | 24 |
| #3 | SE 156-C | 4 |
| #4 | SE 155-C | 24 |
| #5 | SE 124-C | 24 |
| #6 | SE 116-C | 24 |
| #7 | SE 106-C | 24 |

## 6.4 Method Used to Clean 128°F Paraffin from Chips

Most of the paraffin runs off the chip when the carrier is placed on a warm hot plate. At this point, one or all chips on a carrier can be picked up carefully with tweezers and placed in the first cleaning solution. An alternative to the hot plate is heating chips in hot (not boiling) Trichloroethylene (T.C.E.). The cleaning process suggested by Signetics, which is quite standard, is as follows:

1. Decant 3 times in hot (not boiling) T.C.E.
2. Decant 3 times in acetone
3. Decant 3 times in methyl alcohol
4. Dry

A problem in the cleaning step is keeping the chips separated as they are moved back and forth in the solvents. A commercial item, just made available and showing promise, is the Fluoroware Inc. teflon chip carrier H10-01. Each 4" x 3" X 1/2" tray carrier has compartments for chips, each with a drainage hole. The chips can be washed with solvents while separation by a soft inactive material is maintained. Because of its convenience, it is now used for cleaning chips to prevent sharp corners on one chip from damaging the aluminized surface of other chips.

## 6.5 Inspection of Cleaned Chips

It has been the experienced of most users of uncased chips that a certain percent rejects occur due to handling from the time the chips are taken off the line until they are ready for placement in a chip array. Virtually all of these failures are mechanical in nature, such as scratches in aluminization and cracked edges. It is possible, therefore, to inspect the chips for these mechanical failures and cull them out.

All Signetics chips show evidence of two different probings since there are at least two needle scratches on each aluminum pad. One scratch appears to be the normal wafer probe cycle. The other scratch appears to be caused by electrical checkout probes used after die separation. In some cases severe gouging and delamination of portions of a few pads makes a number of the chips unusable.

A few chips also have jagged remains of neighbor chips hanging to one side or another due to imperfect scribing. While this does not bother the I.C. fabricator when he bonds the chips individually into containers, it makes the chip unusable for final beam lead matrix assembly, since the dielectric windows surround the chip in the present concept and such jagged protrusions interfere and prevent proper registration to the beam lead finger pattern.

## 6.6 Method of Shipping for Uncased I.C. Chips

All methods observed for shipping I.C. chips utilize a protective coating of common 128°F paraffin. The use of paraffin demands utmost care in cleaning chips prior to bonding, but appears to be worth it in simplifying the problem of protection while shipping.

It is apparent that the industry has not yet standardized on a method of shipping uncased chips. The method used by ITT Semiconductors Division differed from Signetics. Signetics itself used a different method when shipping chips to ITT Nutley than when shipping to NASA just several months later. Signetics' present method is to mount chips on 2" x 2" x 1/16" thick glass plates with paraffin and then insert the slides into a standard Kodak tray rack 7" long having 36 slots for 2" x 2" glass plates. This adaptation was a reasonable one since the standard Kodak tray provides three layers of cardboard along with sponge rubber for protection of these glass plates in the mails. Several months prior to that, Signetics shipped several hundred chips to ITT Nutley with the chips mounted in paraffin on 1 5/8" square metal meshes made up of 1/32" diameter holes on 1/16" centers punched in metal somewhat heavier than foil for rigidity. Each mesh was placed in a 2" x 3" x 1/2" high plastic box, secured to a plastic surface with double-sided adhesive tape.

The ITT Semiconductor Division method of shipping chips is not satisfactory. Chips are dropped into a small vial or 5 ml. beaker one at a time and a drop of paraffin placed on each one successively. The disadvantage of this method is that upon heating by the user, the chips all drop to the bottom in a pile, scratching one another.

A very satisfactory method of shipment would be a combination of the two Signetics' approaches, namely, 2" x 2" metal meshes mounted in Kodak tray racks. The mesh permits the paraffin to run off when placed on a hot plate. The rugged Kodak box affords shock protection. The chips never touch each other.

## 7.0 PACKAGING CRITERIA FOR TEST VEHICLE

### 7.1 Initially Available Packaging Schemes

The requirements for the test vehicle structure are 125 degree centigrade operation, no greater than 1.25 x 1.25 inches in area, no greater than 200 mils thick, and means for connecting to a mother board.

A number of packaging structures readily available to ITTFL were evaluated as potential candidates for use as this test vehicle structure:

a. A ceramic substrate, ITTFL part CX2309038 having twenty holes near each of two opposite ends.

b. A plastic microcomponent board having molded-in, weld-pin feedthroughs and integral 20-pin connector at each of two opposite ends.

c. A ceramic frame of commercial design having twenty weldable ribbon leads on each of two opposite edges and means for sealing a top and bottom cover plate.

Unfortunately the topology of matrix interconnections described in Section 8, "Layout of Beam Lead Matrix," showed that a regular geometry "universal" or wide usage package was impossible for the proposed test vehicle, so further work on this packaging design was abandoned in favor of an in-house custom design using co-planar leads disposed about the periphery of the container.

### 7.2 Coplanar Package Design (Final Design)

Since the exit points in the Test Vehicle were concentrated in "odd" locations for solving in a high-density matrix, a coplanar design was next chosen. The finalization of this design took some three months of experimentation and is depicted in ITTFL assembly F-2309657.

Preliminary layouts of the beam-lead matrix made early in the reporting period showed that an area of about 1.16 square inches would be required on the substrate to accommodate 42 I.C. chips, over 400 etched conductors and beam leads, and 151 exit nodes. This area breakdown is as follows:

a. Chip area

| | | |
|---|---|---|
| 8 chips (66 x 57) = | | 30,080 |
| 9 chips (48 x 47) = | | 20,340 |
| 9 chips (42 x 48) = | | 18,180 |
| 16 chips (57 x 47) = | | 42,880 |
| | | 111,480 sq. mils |
| | = | 0.111 sq. inches |

b. Finger pattern area (including eyelets)

| | | |
|---|---|---|
| 8 patterns (110 x 90) = | | 79,200 |
| 34 patterns (90 x 90) = | | 275,400 |
| | | 354,600 sq. mils |
| | = | 0.355 sq. inches |

(Area inefficiency through use of short beam leads is thus 0.355/0.111 = 3.15 factor.)

c. Conductor area

1. Area of beam patterns: 0.355 sq. inch
2. Side distance of pattern if square: 0.593 inch
3. Assume average conductor length is one half of pattern square: 0.30 inch
4. Assume etched conductors are equivalent to 3/4 (beam leads + exit nodes)
5. Estimated conductors = 3/4 (486 + 151) = 470
6. Assume conductor spacing = .01 inch
7. Total area of conductors: .300 x 470 x .01 = 1.410 sq. inch
8. Conductor area each side of matrix = 0.705 sq. inch

d. Exit node area:

151 lands (25 x 25) = 100,000 sq. mils
= 0.100 sq. inches

e. Summary of required areas, sq. inches:

| | |
|---|---|
| Finger patterns ---------- | 0.3546 |
| Conductor paths ---------- | 0.7050 |
| Exit nodes ---------- | 0.1000 |
| Total area of matrix -------- | 1.1596 sq. inches |

The above assumptions on average quantity of conductors and the average path length per conductor are based on previous experience with hundreds of interconnection matrices for integrated circuits in flatpack containers. The close agreement of this estimate with the actual area of 1.20 x 1.20 = 1.440 square inches shows that the test vehicle is a typical digital array. Close inspection of the two surface artworks shown in Figure 8-4 and 8-5 reveal that some improvement in surface compactness could have been achieved by re-layout but is not part of the scope of this study.

A one tenth inch thickness of lead sealing walls was allowed around the periphery, making the overall substrate size 1.40 by 1.40 inches. The recalculated power dissipation discussed in section 6. is 750 mw. The same 2 square inches of substrate mounting surface should handle the escape of this heat energy with very little temperature drop, provided the base of the package is intimately connected to an adequate heat sink.

The perimeter of the matrix is 4 x 1.20 or 4.80 inches. At 25 mil spacing for exit ribbon leads (as recommended by E.I.A.) a total of 192 leads can be accommodated around the periphery, or 48 per side. The need for 151 exit leads necessitated use of all four sides of the package. The pin assignments as correlated to the logic diagram E 2309494 (revised Figure 8-2) are included on the assembly drawing.

## 7.3 Multi-Layer Construction

An enlarged cross section detail on the assembly drawing F2309657 shows how the matrix exit nodes are connected to the package ribbon leads. Were the external ribbon leads and the connecting pathways to the integral to the beam lead matrix, there would be considerable simplification of the package for the test vehicle. However, the matrix area would be enlarged by about half of the space used up on the "exit layer" artwork shown in Figure 8-9. (One half on each side of the beam lead matrix). The area of the matrix would then be an estimate of 50 percent larger or 1.50 by 1.50. With the package frame for lead sealing, the result would be a 1.70 by 1.70 size. Not only is this size much larger than the goal set in the study contract, but the overall size would tend to aggravate shrinkage and thermal expansion discrepancies.

It was decided that the exit function would be implemented by a separate level of conductors on a separate laminate called the "exit layer" (item 3 on the assembly print). This layer of conductors is insulated from the surface conductors on the beam lead matrix by an insulating spacer (item 2) having window openings for the chip access and perforations at each exit node so that the two parts can be resistance welded at all 151 congruent points.

## 7.4 Package Ribbon Leads

The enlarged cross section detail on the assembly drawing F 2309657 also shows the construction of the package side wall where the ribbon leads pass through. The ribbon leads are pattern plated integral to the exit layer conductors. This necessitates adding of the side wall package frame after the internal microassembly is complete.

In the zone where the ribbon leads are to pass through the side wall, the dielectric is digested away in the form of a moat. (See Figure 8-12 for this pattern of dielectric cutting). This technique provided to be quite successful. A margin of dielectric is retained around the periphery of the exit layer which anchors down the ends of all ribbon leads so that they can be precisely located and attached to the next higher assembly.

## 7.5 Summary of Chosen Package Physical Parameters

The final package design has the following features:

1. Container size: 1.40 x 1.40 x 0.125 inches
2. Gross mounting area: 1.60 x 1.60 inches
3. External pin capability: 192 leads
4. Usable area for matrix structure: 1.44 square inches

5. Usable area for chips: 120,000 square mils
6. Percent of gross area used for external leads: 23.5%
7. Percent of gross area used for package seal: 20%
8. Precent of gross area used for etched conductors: 38.8%
9. Percent of gross area used by beam leads: 9.5%
10. Percent of gross area used by exit nodes: 3.9%
11. Percent of gross area used by I.C. chips: 4.3%
12. Including added 1/16 inch p.c. board, system density of I.C. chips: 84 I.C./ cu. in.

## 8.0 TEST VEHICLE REQUIREMENTS

### 8.1 Logic Diagram

The logic diagram for the test vehicle is shown in Figure 8-1. This subsystem receives a controlled chain of clock pulses and by means of four binary counter/dividers and sixteen 4-input line drivers, develops pairs of signals to drive eight banks of electro-mechanical switches remotely located.

Each bank of switches contains 16 paralleled SPDT switches, making a total of 128 switches which must be examined. The large quantity of switch lines are received in a cable from the remote location where they enter sixteen sets of eight input OR gates. The original clock is further divided by four additional binary counter/dividers and coded into sixteen slow, sequential enabling gates. The fifth input to each enabling gate is the inverted signal from the OR gates.

A wide fan-in gate combines all resulting signals into a sequential chain of pulses where the polarity of each sequential square wave indicates the status of each switch, either in the normally closed condition or tripped into the abnormal state.

The subsystem uses the chips listed in Section 6 on Silicon Integrated Circuit Chip Technology as Table 6.1.

### 8.2 Engineering Layout of Beam Lead Matrix, Regular Geometry

Considerable trial and error effort was expended in an attempt to provide a successful two-sided matrix solution using a geometrically regular array of exit nodes. Any proposed packaging scheme using axial leads would require such a regular array of exit nodes against which the header pins could be bonded. An arrangement of seven rows of 23 exit nodes on 50 mil centers was used to provide a capacity of 161 exit points. The test vehicle requires 151 exit points, so there would be 10 spare nodes not used for exit purposes.

After about one man week of layout effort it was concluded that the topology boundaries for 128 of the exit nodes were concentrated into one small zone of the matrix and were being blocked by the parallel rows of exit nodes. Present chemofacture technology capability prohibits more than 2 conductors to pass between exit nodes spaced on 50 mil centers. This limitation creates a "dam-effect" and apparently there is no possible solution to the interconnection paths when such a limitation is combined with the restriction of two layers of interconnection.

Proposed packaging shown in ITTFL parts C2309569 and D2309600 had to be abandoned when it was concluded that a peculiar and unique placement of the exit nodes was required to satisfy the requirements. Since a unique package design could not be justified as a vendor-procured part, it was decided to proceed with a co-planar packaging design which could be fabricated within the capabilities of the Microelectronics Department. The details of the co-planar package approach are described in section 7.

### 8.3 Engineering Layout of Beam Lead Matrix, Unique Geometry

From the experience gained in the failed layout using regular geometry, a unique layout was quickly determined using the exit node pattern depicted by ITTFL layout

F2309642. This pattern concentrates the 128 nodes concerned with the signals from the switches into double rows of points arranged as close as possible to the two rows of chips on the left of the matrix, which are the diode logic-isolation chip functions.

The other consideration in placement of chips was to arrange the eight type SE 155C line drivers close to one edge of the matrix since they are high-dissipation dual line drivers and should not be die-bonded onto the substrate in the central region of the matrix where the hot spot temperature would be aggravated. Additionally, these chips generate a set of 16 output signals which are less "blocked" in the layout if these exit points are at one edge of the matrix.

The solving time for the beam lead matrix was about four working days for a designer having moderate previous training in competitive path solving using only two surfaces for conductors.

The resulting solution is depicted on ITTFL layout F2309642. This layout exhibits the following statistics:

| | |
|---|---|
| Number of I.C. chips | 42 |
| Number of active beam lead bonds | 494 |
| Average bonds per I.C. chip | 11.7 |
| Number of exit bonds | 151 |
| Total number of man-made bonds within the test vehicle | 645 |
| Number of "extra" free use eyelets | 115 |
| Total number of plated feed-throughs in use | 472 |
| Overall number of plated feed-throughs | 760 |
| Number of separate signal and power networks | 215 |
| Equivalent etched interconnection path segments | 463 |

The extra free-use eyelets were required to cope with the congestion caused by the input and output binary code data bus lines, there being eight parallel lines in each data bus which require taps at all 16 possible binary combinations of four flip-flop outputs.

## 8.4 Graphic Engineering of Beam Lead Matrix

Several levels of precision were required to form the processing artworks for the beam lead matrix; finger patterns, conductors, feed-through, and tool artwork. These levels of precision are discussed below:

8.4.1 Finger Patterns. Seven types of beam lead finger patterns were scribed. These patterns require spacing accuracy of about 1/4 mil or 250 microinches in order to be congruent to the aluminized lands found on the Signetics I. C. chips. The coordinatograph scale chosen was 100 to 1. A ten-to-one reduction was made to produce the 42 finger pattern transparancies required on the surface artwork at ten-to-one scale. A centering target was placed on the center lines of each beam lead finger pattern to facilitate later alignments to the surface conductor artwork. This mark falls out during chemofacture.

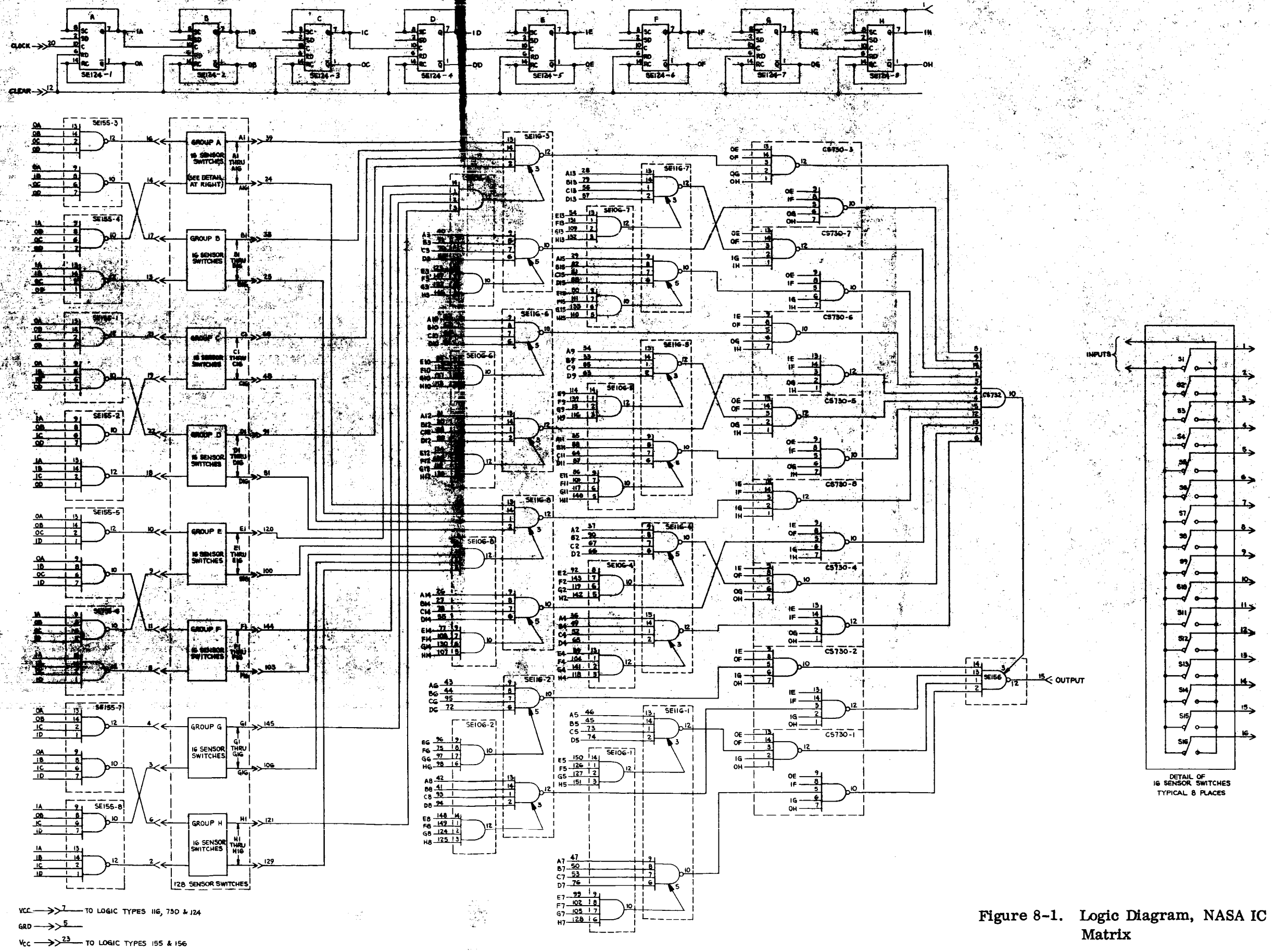


**Figure 8-1. Logic Diagram, NASA IC Matrix**

The flip-flop I.C. as shown on ITTFL drawing A2309632,"Positioning Diagram for Chip Type SE124-C" is considerably larger than the other chips. As a result, the plated eyelets centers which anchor each beam lead fall on a rectangle 80 by 100 mils. All other chips fall within a square outline of eyelet centers 80 by 80 mils, such as depicted by the positioning diagram for the SE 155-C, ITTFL drawing A2309633. The compactness of these included areas reserved for the chip occupancy and the beam lead functions permitted the array of 42 chips to be included in an area of 1.200 by 1.200 inches. This local density is about 29 integrated circuit chips per square inch compared with about 6 integrated circuits per square inch using flatpack cases, or an improvement of almost five to one.

8.4.2 Conductor Artwork. Although the layout was made at twenty-to-one the taped masters were cut at a ten-to-one enlargement, primarily because of span limitations on the coordinatograph. An accurate master of all exit nodes per F2309599 was scribed at ten-to-one. The "extra" 115 feedthrough holes were then cut on a separate master. The two types of photo-reduced chip eyelet lands were cut at 100:1 and photo-reduced to ten-to-one. Then eight copies of the 100 x 80 mil pattern and 34 copies of the 80 x 80 mil eyelet pattern were "dubbed" onto the exit nugget pattern. The composite master was then contact printed twice, one for a top master, the other for the bottom master.

The top master then received the 42 finger patterns in various quantities of seven types. Finally the top and bottom masters were taped with 50 mil tape, following the layout diagram. The taping and cross checking took about 30 man hours, since there are more than a thousand segments of tape to be placed and cross checked on the two surface sheets. Finally, these taped masters were photo reduced to true size. This results in beam lead widths as narrow as three mils and surface conductors of five mils in width.

8.4.3 Feed-Through Artwork. Three masters were required for the 76- feed-throughs put into the beam lead matrix, one with 5 by 5 mil cutting holes, one with 151 square 20 by 20 mil exit lands, and one with the 10 x 10 mil lands for all beam lead eyelets and the variously located "extra" feed throughs for signal paths. To save labor, two of these masters were composites, since the beam lead finger eyelets exhibited a highly repetitive pattern.

8.4.4 Tool Artwork. Various access opening "windows" are required for the I.C. chips as well as a perforated outline to permit accurate removal of the scrap laminate boarder. The four precision pins used for microassembly purposes are 40 mils diameter. The cutting diameter of these tool holes was determined to be 35 mils diameter to permit undercutting enlargement and retain a slight interference fit with the four 40-mil alignment pins.

8.4.5 Flow Diagram of Beam Lead Matrix Graphics. A flow diagram of the graphics engineering required to generate fabrication photo-transparencies for the beam lead matrix is shown in Figure 8-2. All told, 14 basic scribe patterns were cut on the coordinatograph. The "dubbing-in" for local somewhat repetitive details was required in order to achieve accuracy. The two patterns of extra feed throughs (cutting and plating) could have been combined with the exit node patterns, but the exit nodes alone required for the insulating separator and the exit traffic laminate brought about by the unusual complexity of the test vehicle, so these patterns were kept separate to save on extra scribing labor.

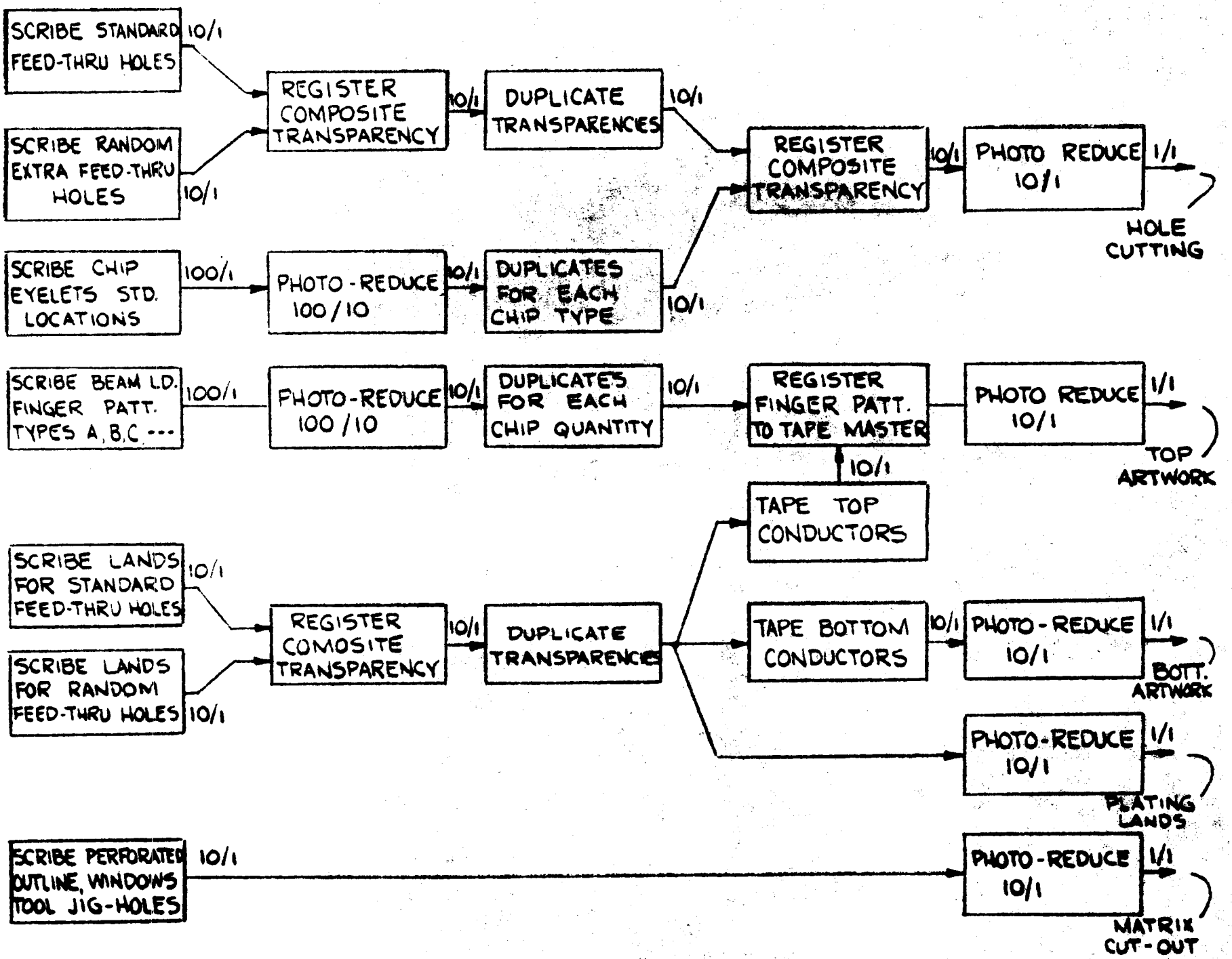


**Figure 8-2. Flow Diagram of Graphic Composition**

## 8.5 Graphics Engineering of Exit Layer

As reported in Section 7, "Packaging Criteria for the Test Vehicle," the complexity of the 42-chip array required an exit layer to be developed. This exit layer is a single-sided pattern, but because it requires opposed tip resistance welding, the 151 exit nodes were of the feed through type, requiring the use of pairs of registered transparencies.

The exit layer is made more complex in that the exit tabs (made of pattern-plated nickel) required suspension across an area where all of the dielectric was digested away. Because of the shape around the periphery of the exit layer, it is called a "Moat." During the final packaging, an epoxy seal is made along the inner portion of the moat to seal out humidity. Where the exit tabs extend beyond the seal, they become the outside world ribbon lead connections, being integral to the welded exit nodes on the interior of the package.

## 8.6 Use of Flexible Transparencies

Throughout the graphics engineering, the working transparencies used in the various chemofacture processes were stable base flexible cut film. All registration was made with an optical loop and checked on an optical comparator accurate to 100 microinches.

Care must be taken that the master layouts, camera, dark room chemicals, and product exposure cycles are all at the prescribed temperature in order to retain congruency of patterns in four to five exposure cycles. Some of the beam lead artwork, where detail was accurate to about 100 microinches, did not expose accurately if the feed through eyelets were built up prior to the surface artwork cycle. It was hoped that the flexible transparencies would conform to the laminate when placed under the vacuum of the exposure frame. However, the square outline of eyelets (80 x80 mils) prevented an emulsion-to-emulsion condition to prevail, causing distorted beam lead shapes. Exposing the surface beam lead pattern prior to eyelet buildup avoided the problem. The same sequence of chemofacture could be used, therefore, for rigid glass plates, but no experiments were conducted to determine the effects of glass plate transparencies.

Copies of all precision transparencies are shown at about 3.75 times larger than true size in Figures 8-3 through 8-13.

## 8.7 Laboratory Construction of Test Vehicle

The construction of the test vehicles required large amounts of repetitive experimentation to develop a usable product. The phases of experimentation are as follows:

a. Chemofacture of the beam lead matrix, the exit layer, and the insulating spacers.

b. Fabrication of tooling jigs to permit registration of the above items into a single welded subassembly.

c. Fabrication of alumina substrates and development of die bonding the I.C. chips into accurately determined positions.

d. Development of ultrasonic bonding understanding including tip shapes and vacuum fixturing to hold the chip array in place, registration to the welded subassembly of beam leads and exit layers, and the properties of the beam-lead structure which lead to good bonds.

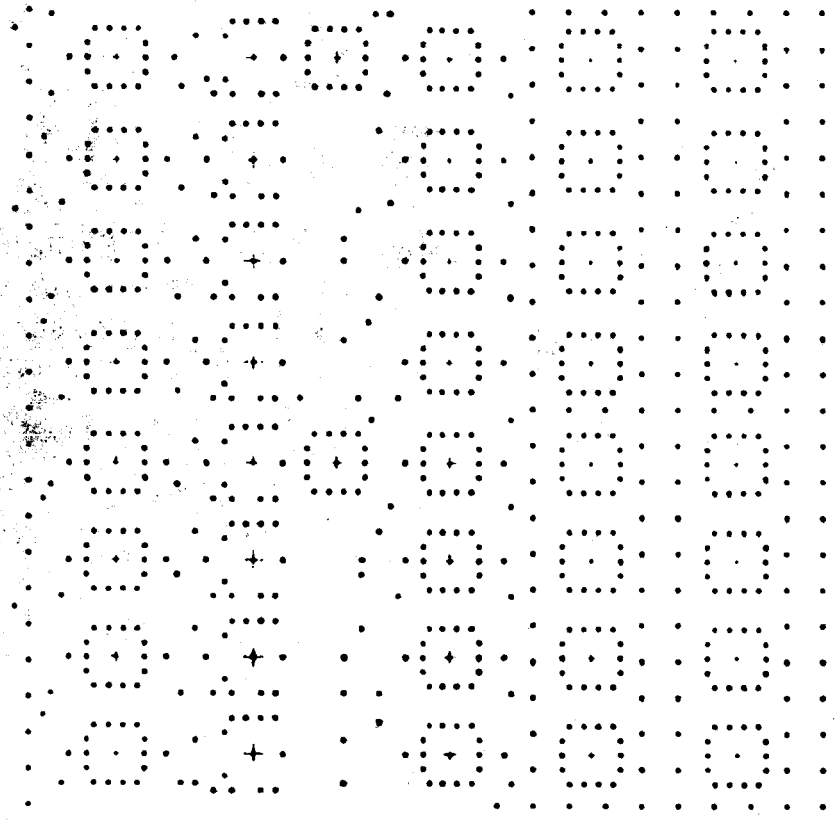

Figure 8-3. Beam Lead Matrix: Cutting Holes (5 mils)

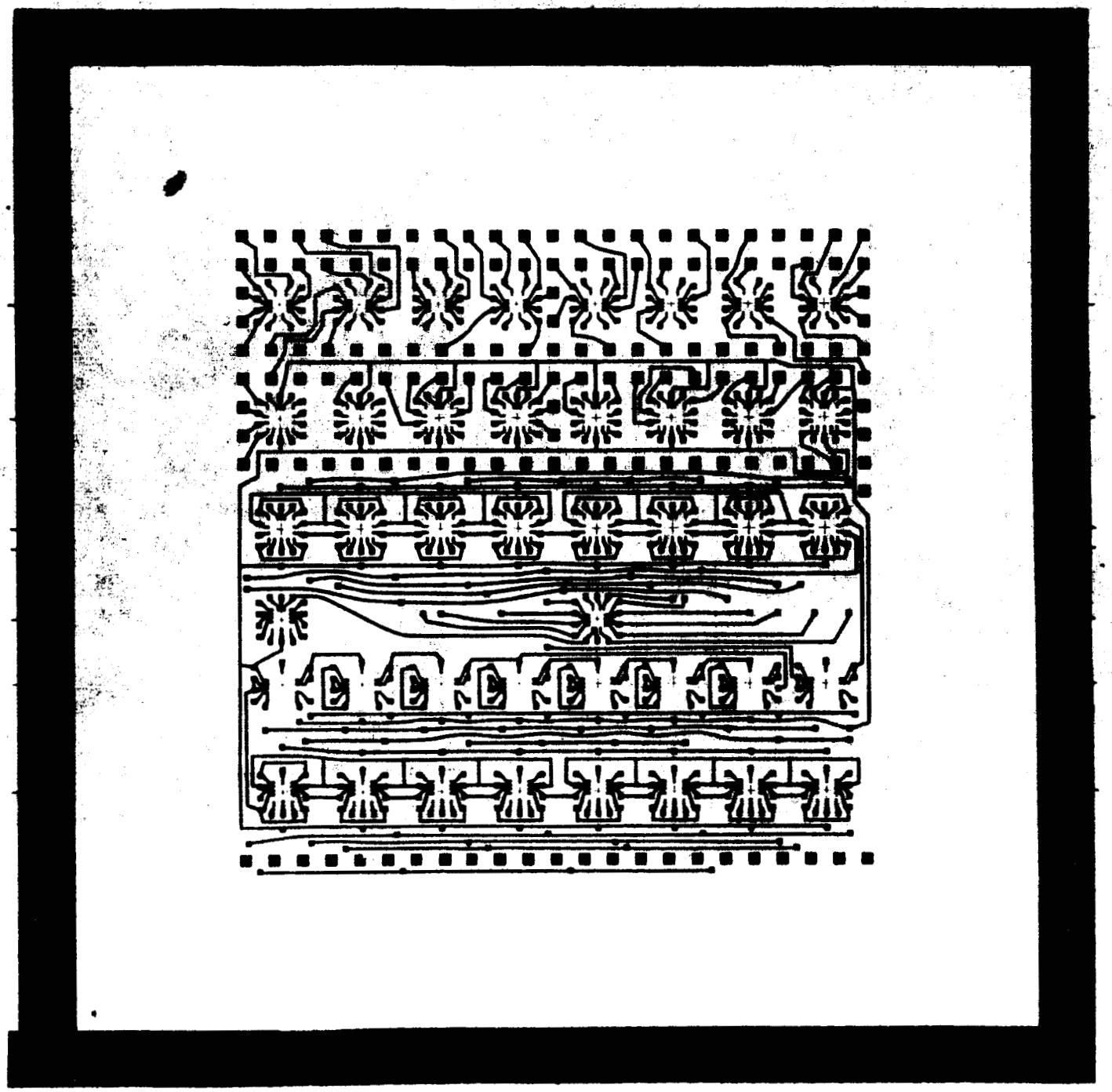

Figure 8-4. Beam Lead Matrix: Top Surface Conductors

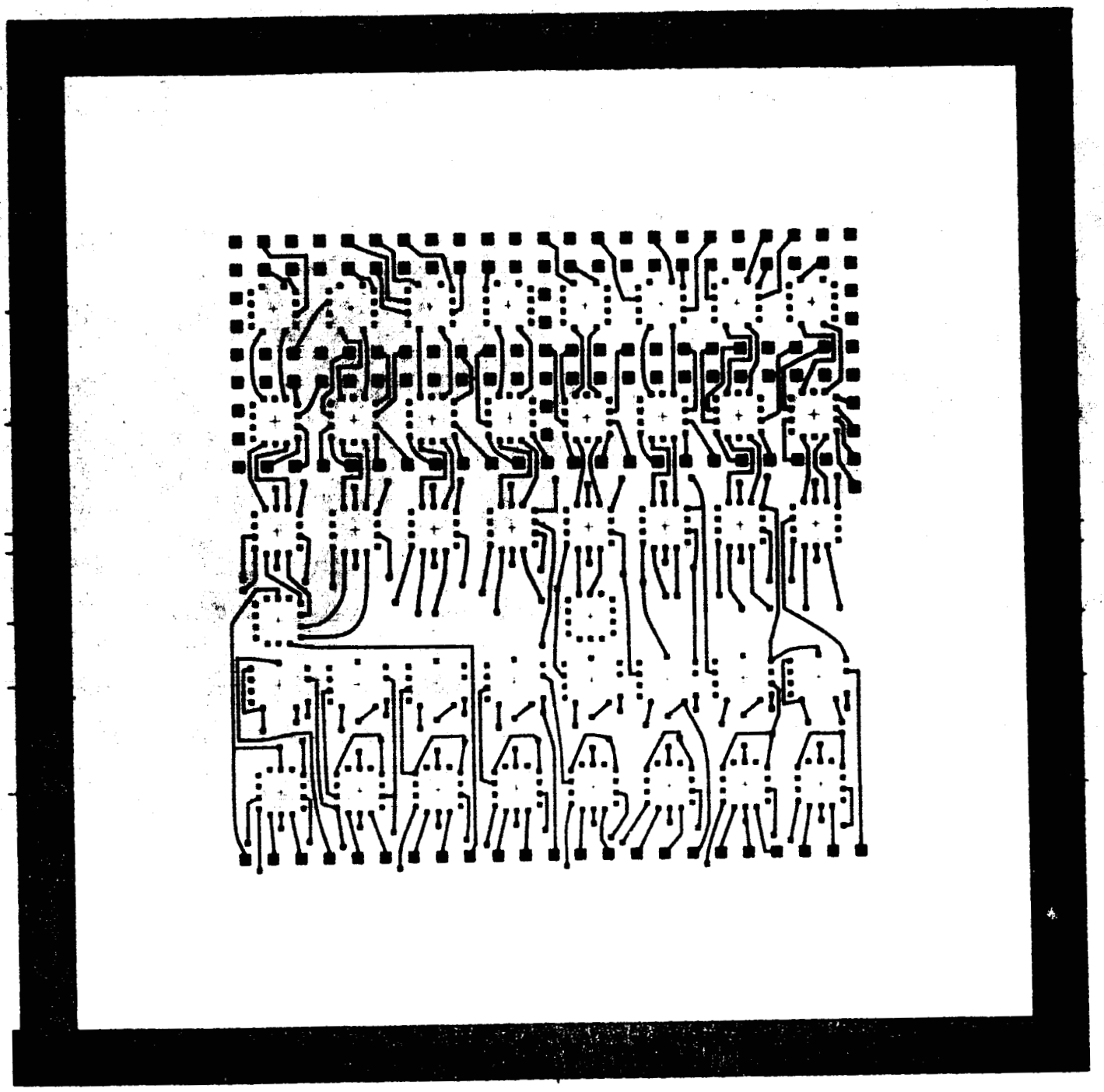

Figure 8-5. Beam Lead Matrix: Bottom Surface Conductors

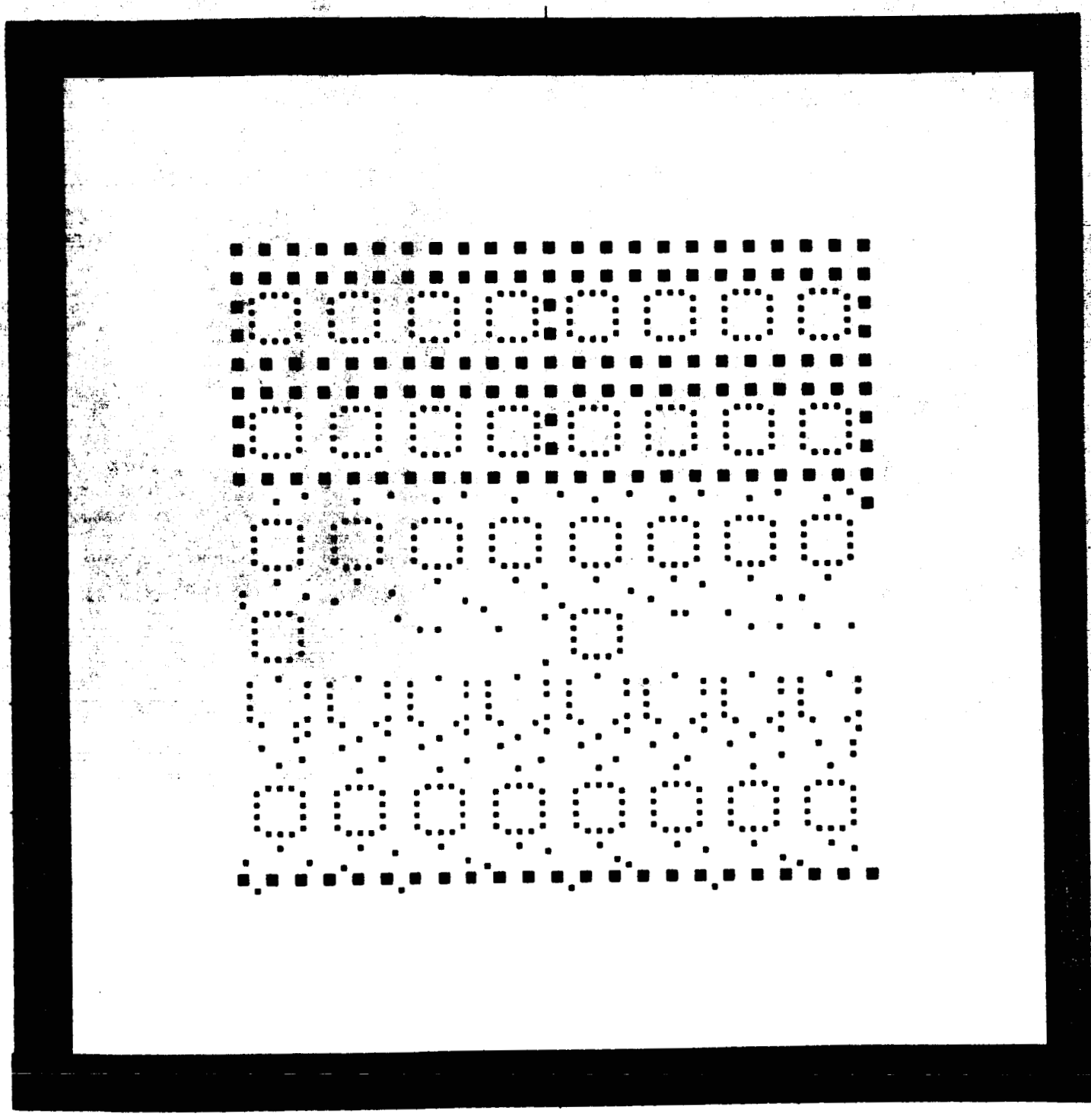

Figure 8-6. Beam Lead Matrix: Feed-Through Plating Lands

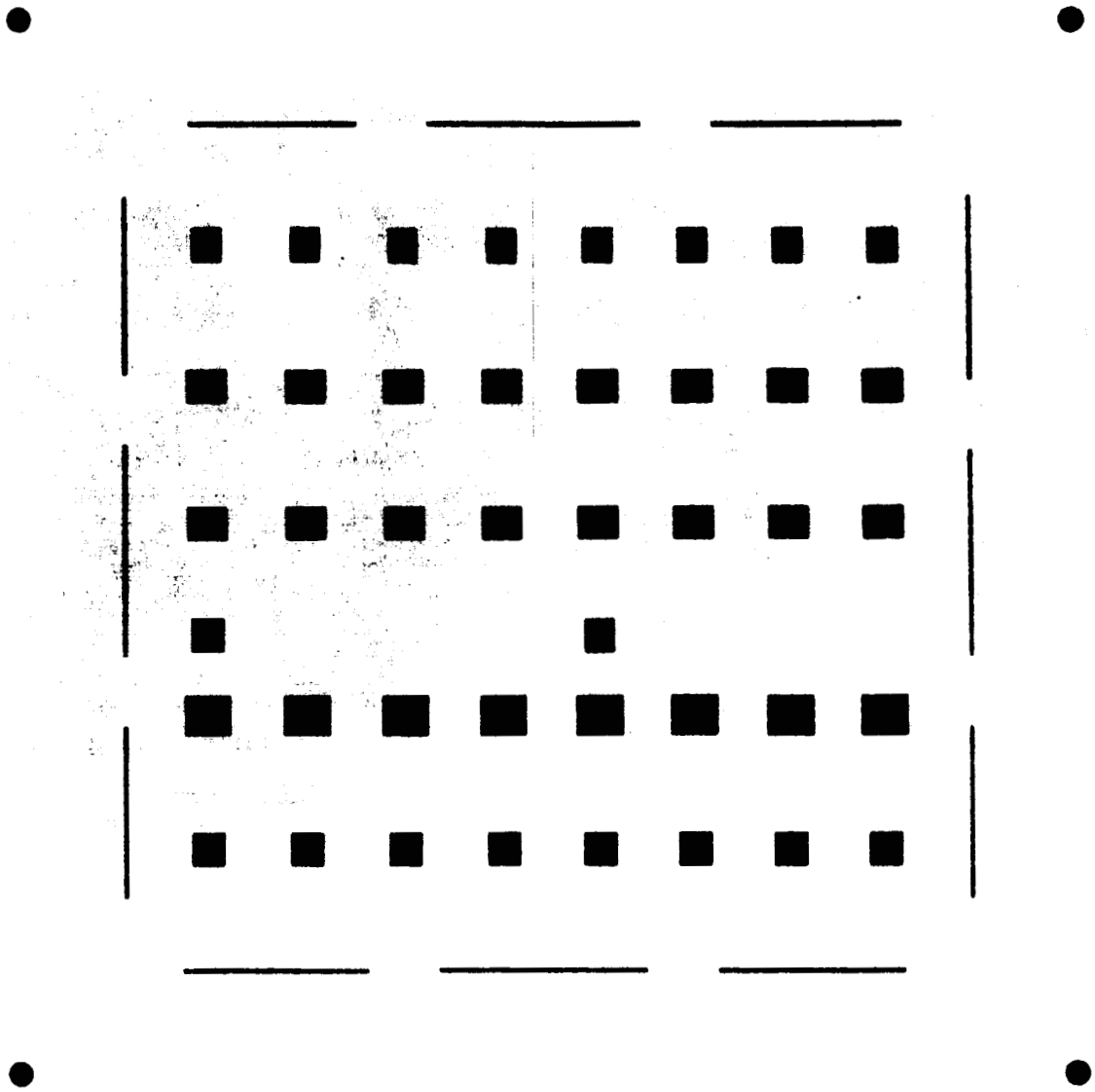

Figure 8-7. Beam Lead Matrix: Chip Windows & Jig Holes

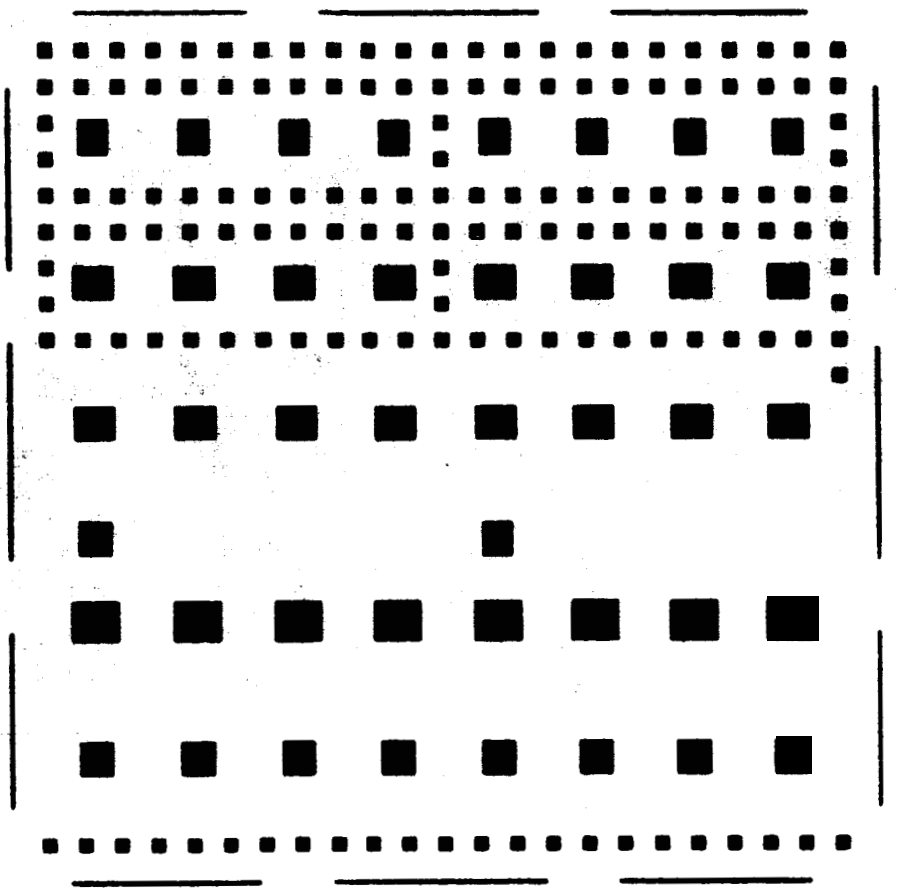

Figure 8-8. Insulating Separator: (Between Matrix & Exit Layer)

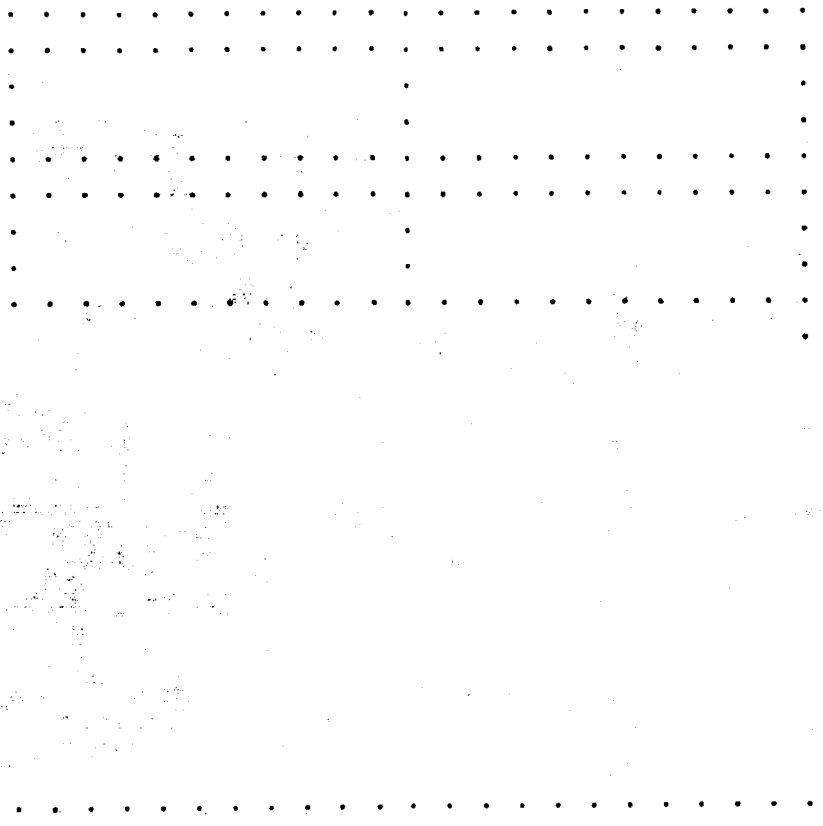

Figure 8-9. Exit Layer: Cutting Holes (5 mils)

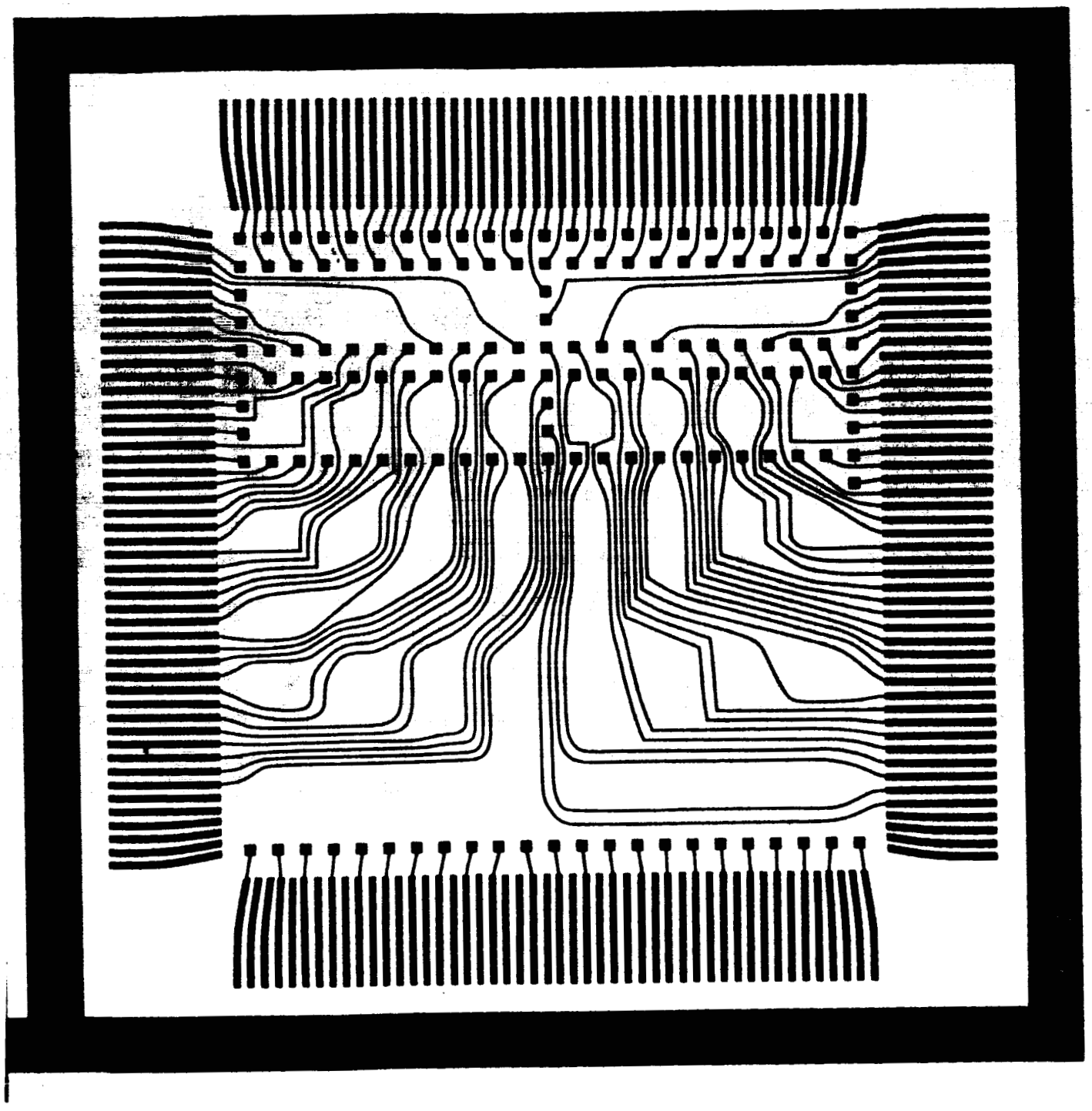

Figure 8-10. Exit Layer: Surface Conductors

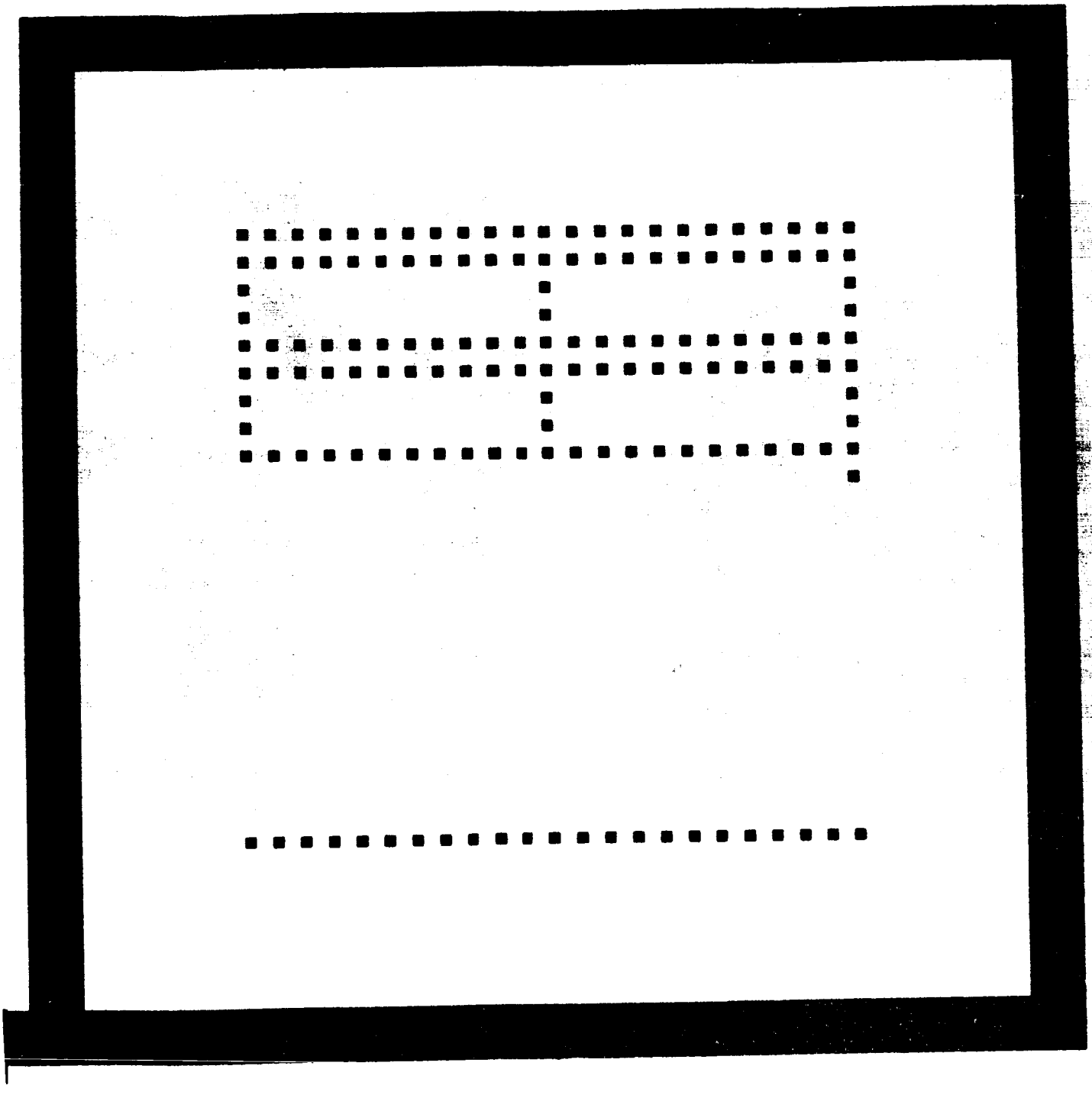

Figure 8-11. Exit Layer: Feed-Through Plating Lands

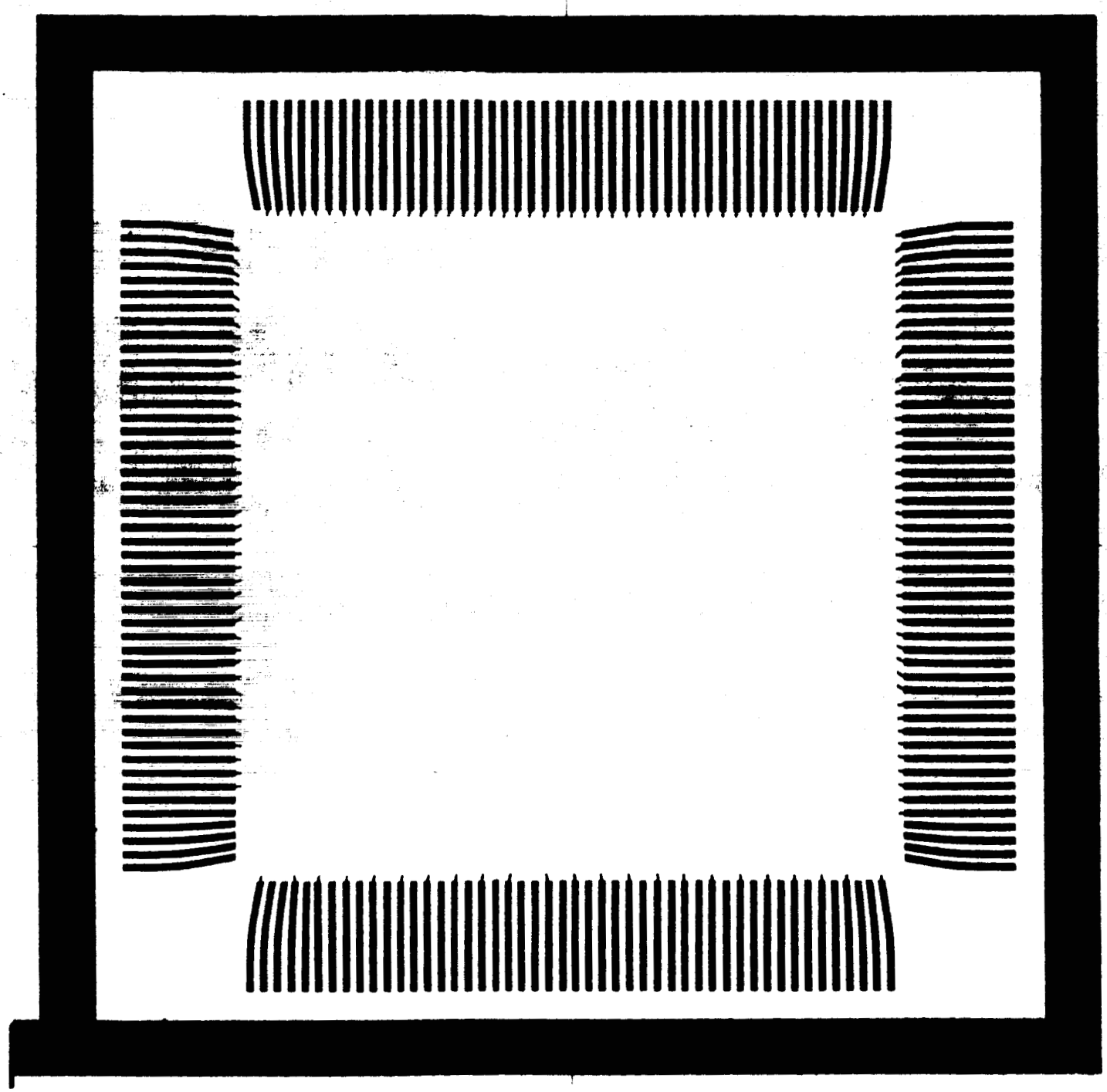

Figure 8-12. Exit Layer: Ribbon Lead Build Up

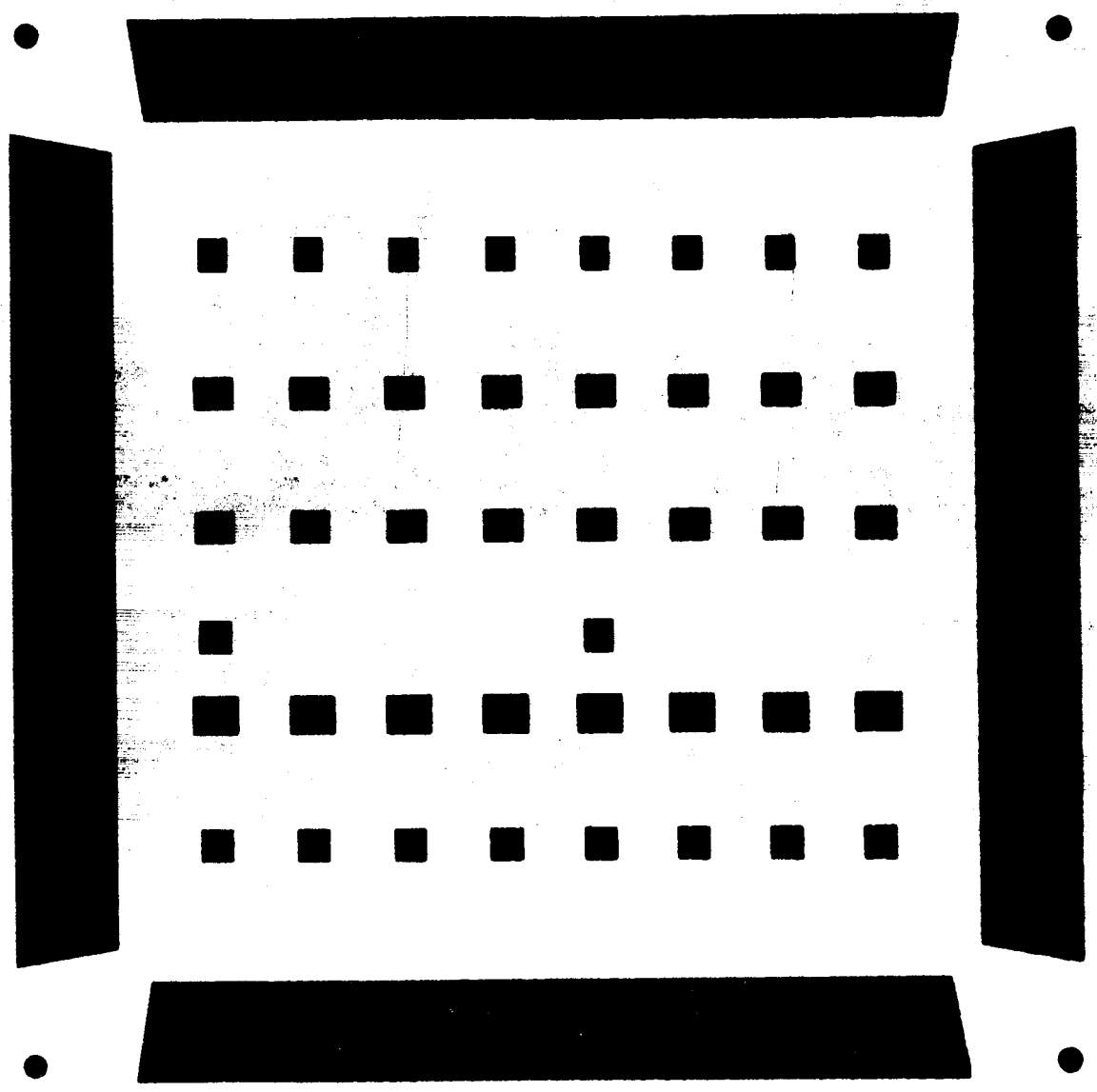

Figure 8-13. Exit Layer: Chip Windows, Moats Tooling

e. Development of casting molds to fabricate test vehicle package enclosures.

f. Encapsulation techniques for silicone gel and container sealing.

g. Design and fabrication of test p.c. boards and connectors to permit electrical checkout of the test vehicle.

h. Design and fabrication of sturdy fixturing to hold the test vehicle and test board during the stringent environmental testing cycles.

8.7.1 Chemofacture of the Beam Lead Matrix, the Exit Layer, and the Insulating Spacers. This subject is discussed in section 3. In order to obtain significant data, six sets of all transparencies were used so that batches of six parts could be made at one time. During the third reporting period, over thirty beam lead matrices and eighteen exit layers were chemofactured.

Three types of beam lead matrix, ITTFL part B2309660, were made having fine detail finger patterns: all copper beams, all nickel beams, and copper beams with nickel-clad tops. Two types of feed through were tried: soft watts nickel plated holes, and watts nickel with a build-up of bright "leveling" nickel overplate.

8.7.2 Fabrication of Welding Fixture. Two welding fixtures, ITTFL part B2309667, were made. These open frames contain four steel pins 40 mils in diameter which are located by means of precision artwork. The camera work had to be repeated at a reduction scale oversize by about one percent so as to cause a "curtain-stretcher" effect to keep the laminates taut while the opposed tip welding is being performed.

8.7.3 Fabrication of Alumina Substrates. This part, ITTFL B2309664, is 1.40 by 1.40 inches. The substrate is cut with a diamond saw from 25 mil stock, American Lava Corp., 95 percent alumina content. About sixteen have been fabricated and used in various assembly experiments.

8.7.4 Development of Ultrasonic Bonding. The bonding per se is discussed in section 2. When the beam lead fingers were made to be compatible with the Signetics DTL I.C. chips, the resulting beams were about 3.5 mils wide and 1.5 mils spacing. Special tool tips were required which are modifications of ITTFL part C2309484.

A jig with the four registration pins was required for the 42 chip array so that a typical beam lead matrix could be placed over the chips while they were being slid about on the soft die bonding cement. After oven curing of the die bonds, this typical matrix was taken off and the intended subassembly of welded exit layer and beam lead matrix registered by means of the same pins. This assembly jig is represented by B2309649 and is similar to the weld jig except for lack of an access opening as required for the opposed tip welding.

In the experiments on mylar matrix shrinkage at 175°C, it was determined that differential shrinkage was not repeatable to within 1/2 mil as is necessary for exact beam lead registration. Therefore, a typical matrix could not be used as a chip positioning reference and the assembly jig then became unnecessarily precise for mylar-base laminates.

Considerable trouble was experienced in the performance stability of the original ultrasonic bonder. The generator was a vacuum tube model and overheating tended to cause drifting of the 60 kHz power oscillator. The magneto-strictive transducer also exhibited

drift in the resonant frequency, apparently from room temperature changes, alteration in D.C. magnetic bias, or pulse duty cycle as the bonder was used again and again. In addition, it was discovered that power supply voltage had to be maintained at ± 1V. These difficulties confounded the analysis of the consistency and repeatability of various experiments using different metals for the beam leads. Three trips were made to the ultrasonic bonder manufacturer to maintain operation.

Consistency was achieved when ITT purchased a new solid-state swept oscillator generator. This new generator circumvents the changing resonance of the transducer by sweeping back and forth over a range of frequencies beyond the possible drift limits of the transducer at an audio repetition rate.

8.7.5 Test Vehicle Package Enclosure. The plastic frame was made as a brass model and a negative RTV mold was made. A mineral-filled epoxy resin was cast in the mold to form the package frame.

Amines given off by the molded frame can cause problems within the package interior, so a thorough bake-out at elevated temperatures was used to avoid such situations. A liquid epoxy seal was first attempted as a package lead seal for each of the four sides of the frame where 48 nickel ribbon leads protrude.

This package assembly idea failed to give trustworthy results. A pair of gaskets made from a sheet of "B-cure" epoxy was finally chosen as a lead seal. Using a suitable weight for pressure, the "B-cure" epoxy gasket reflows at a high oven temperature, forcing the material around all 192 exit ribbon leads disposed about the edges of the package.

8.7.6 Encapsulation Techniques. The test vehicle must withstand severe environmental stresses. Analysis of the results of testing require access to the 42 chip array within the test vehicle package. Thus the cover of the package had to be left off introducing possible hazards from moist, contaminated air.

A silicone gel encapsulant was chosen as an encapsulating medium. In the catalized state it is a thin liquid with a property for "wetting" or adhering to most materials, including all those present in the study vehicle. Thus, pouring this gel liquid onto the assembled chip array was quite successful. The liquid gel works into all crevices, but the complexity of the matrix and exit layer welded structure traps some of the air bubbles. A light vacuum and a heated cure cycle above 175°C provides an encapsulant having the consistency of gelatin dessert. The water clear get permits microscopic examination without any difficulty. Electrical probing can be done successfully through the gel since it is self-healing.

8.7.7 Test Board Fabrication. A test board having the capability for connecting four p.c. receptacles was designed to permit examination of the 151 exit terminals during electrical checkout. The most compact receptacles for the 1/16 inch thick p.c. board required to survive vibration and shock tests has contacts on 50 mil centers, so each side of the test board has to be at least 3.5 inches on a side. The design is depicted by ITTFL artwork F2309261-9.

8.7.8 Environmental Test Fixture. Only the interior of the test vehicle is under examination during the severe shock and vibration testing. However, the delicate exit leads necessary for the high density requirement imposed on the test vehicle necessitated the use of a rather rugged set of metal parts. These fixture parts prevent movement or flexing of the exterior parts of the package or the p.c. test board and its cables.

## 8.8 Excessive Complexity of the Test Vehicle

The complexity of the test vehicle is far greater than had been anticipated. The quantities of beam leads and feedthroughs in a single matrix are statistically significant, however, and considerable insight into yield factors and laboratory type manhours to construct each matrix or exit layer has been gained, as well as timing factors to die bond and ultrasonically weld the beam leads.

Among the features which complicated the study are:

a. Time consuming efforts were expended toward development of an adequate packaging scheme which could handle 151 signal terminals. The choice of ribbon leads on 25 mil centers is in keeping with recent thinking in the EIA committees on Micro-Electronics Devices (M.E.D.)

b. A complete set of additional precision artworks was required to enable "topology escape" of the 151 signals from the beam lead matrix.

c. The performance features of the feed throughs which are used for "exit" purposes required additional development so that they could withstand the stresses imposed by the opposed-tip resistance welding required to join the beam lead matrix to the exit layer.

d. A weld schedule had to be developed which would join a pair of stacked hollow eyelets, 151 places in the matrix.

e. An extra insulation layer was required to prevent electrical shorts between the matrix and the exit layer as well as a special welding fixture for the sub-assembly prior to die bonding.

f. The quantity of exit pins necessitated a rather bulky test board and cable connector system so as to withstand the rigors of the envirnomental tests.

## 8.9 Description of Finalized Microassembly Procedure

The final scheme chosen for microassembly is as follows:

a. Weld together the beam lead matrix and the exit layer, with a separator of perforated Mylar insulation between them. All 151 exit nuggets are opposed tip resistance welded while held in registration with the weld jig. In effect, this welding creates a three-layer matrix.

b. The sub-assembly matrix is heat shrunk for two hours at +175°C held supported in the weld jig with 2 pounds of distributed weight to confine the matrix to a flat plane.

c. A ceramic substrate is temporarily set into the recessed bonding jig and a positioning plate is set over the substrate to loosely position the I.C. chips.

d. A small hemisphere of freshly prepared silver-epoxy cement about 10 mils in diameter is placed in the center of each chip mounting spot.

e. The cleaned and inspected I.C. chips are oriented and placed on the spots of cement.

f. The heat-shrunk matrix sub-assembly is fitted on the jig pins and the chips are pushed down into the cement spots and positioned into registration under the finger patterns of beam leads.

g. After 1 hour of resting time to permit the I.C. chip cement to set, the matrix is taken off and the substrate with chips is oven cured for 1 hour at +175°C.

h. A package gasket of B-cure epoxy film is placed around the periphery of the substrate and the trimmed matrix is again placed in registration with the chips.

i. The beam leads are bonded to the chips - all horizontal, then all vertical.

j. A second package gasket is placed around the periphery and the molded package frame is positioned over the gaskets.

k. Under heat and pressure, the package frame is sealed to the substrate boarder and the B-cure material forms a cured epoxy lead seal.

l. After a bake-out cycle, liquid silicone gel is poured into the interior until nothing breaks through the surface of the liquid. A mild vacuum is applied to get out minute air pockets.

m. The gel is cured for 1 hour at +175°C.

n. The encapsulated structure is transferred from the bonding jig and the base of the substrate is cemented with silver epoxy cement to the central heat sink in the p.c. test board, making sure that the exit ribbon leads register with the etched conductor pattern on the test board.

o. The ribbon leads are parallel tip welded to the test board.

## 8.10 Final Items Constructed

Three items were constructed after the experimental phases were completed:

a. A bread-board test vehicle having 16 chips.

b. A final deliverable 16 chip array on which the environmental tests were performed.

c. A final deliverable 42 chip array delivered without environmental testing.

Each of these items was cemented to the heat sink within the I.C. test board. The test board then becomes an unofficial part of the apparatus which is necessary to handle and perform electrical checks. The 16-chip array also has the environmental test fixture items associated with it.

## 8.11 Conclusions for Packaging

The packaging enclosure should be changed to an inorganic substance so that there is no interaction with the silicon gel and to minimize the differential thermal expansion to the other materials.

The insulating film should be changed to Kapton or a similar dielectric to minimize the shrinking problems.

The packaging enclosure should include built-in registration means to assist in locating the I.C. chips and the beam-lead matrix.

The chemofacture of the exit ribbon leads should be altered to improve the thickness and resiliency of the exit ribbon leads.

The package design should be made compatible to the principle of some of the I.C. flip-chip bonding machinery so that efficient means for registration of the beams to the chip lands can be employed.

## 9.0 ENVIRONMENTAL TESTS OF OPERATING ITEMS

### 9.1 Simplification of the Test Vehicle

Because of the large delays and the technical difficulties experienced in the attempts to perfect the processing and microassembly techniques for the complex test vehicle detailed in Section 8, a decision was made to perform environmental tests on only a partially assembled item having less than 25 operating I.C. chips. The most meaningful section of the test vehicle was determined to be the chain of eight RST flip-flops which divides the clock frequency by 128 times and the eight dual line drivers which are sequentially driven by the 16 possible binary combinations of the first four flip-flops in the divider chain.

The complexity of the beam lead matrix area serving these 16 chips is quite high and any electronic failures can be rapidly diagnosed when analyzing the reason for failure.

Practice chips were installed here and there in the remainder of the beam-lead matrix. These extra chips serve to establish the design center for ultrasonic bonding parameters and they also serve to mechanically secure the matrix to the substrate on overall basis so that there is a realistic mechanical structural situation when performing thermal expansion and shock or vibration tests. In order to prevent these practice chips from interfering with the operation of the 16 chips under test, the power supply circuit to the unused portion of the matrix was cut open.

### 9.2 Required Environmental Tests

The test vehicle is required to operate through the following tests, which are sequentially arranged in the presumed increasing order of severity:

a. Temperature environment: -55 to +125°C

b. Non-operating thermal shock; -55 to +175°C

c. Impact tests, 200 G, 5 millisec in 3 axes.

d. Vibration, 20 to 500 cps at 20 G sweep, also
500 to 3000 cps at 50 G sweep,
sweep rate of 4 octaves per minute,
Vibration tests shall be made in 3 axes.

In the temperature tests the digital operation can be watched closely as the chamber temperature is altered. The dynamics of the other three tests required that the 23-lead test cable not be in place, so these tests were non-operating with functional operation being checked after the test is over. A test machine could not be located which could provide 20G sweep at 20 cycles, so the test requirement was altered from 20 to 22 cps to provide maximum available G sweep and then from 22 to 500 cps the required 20 G was applied.

## 9.3 Preliminary Assembly and Test Results

To gain experience, a preliminary 16-chip arrary was assembled and some of the environmental tests were run on it to determine where alterations to the construction details could be made. The preliminary test item was built using the breadboard I.C. chips brought earlier by ITT and is not considered to be a deliverable item. Prior to testing, the test item had to be subjected to two periods of one hour processing cures at +175°C for encapsulating purposes.

9.3.1 Temperature test. Four cycles were run with the test item in a chamber from +25°C to +80°C with external monitoring of signals. Testing terminated each time at 80°C due to the opening of the external clock nugget weld because of thermostatic action in the diverse materials. Upon cooling to 79°C, the connection would close again. This effect was repeatable before and after impact and vibration tests.

9.3.2 Impact Test. the test-item assembly was given one impact test in each of its three axes. The shock was a rising sawtooth of acceleration, from 0 to 209 G in 3.5 milliseconds and then dropping to 0 by 5 milliseconds. Signals were not monitored during test and the test item was clamped in the environmental test fixture apparatus, ITTFL D2309699 as described in paragraph 8.1.9.8.

9.3.3 Vibration Test. The test item assembly was vibrated through one sweep of 20 to 300 cps on each of three axes. The sweep rate was four octaves per minute. The acceleration was 18 G from 20 to 22 cps; then 20 G from 22 to 500 cps; then 50 G from 500 to 3000 cps. Signals were not monitored during the test and the test item was clamped in the environmental test fixture apparatus.

9.3.4 Results from Preliminary Environmental Tests. The test item was known to have a number of poor weld connections between the double-sided, beam-lead matrix and the exit layer which were traced to inadequate plating of through-holes in the exit layer. The test item was also known to have had an inadvertent stress in one corner of the matrix traced to improper procedure for sealing the side wall to the substrate. The test item also had 10 faulty and rebonded beam leads plus 1 beam lead which was attached by silver epoxy cement since ultrasonic rebonding could not be achieved.

a. Temperature - two beam leads opened.

b. Impact - One beam lead noted to be squashed by a slipped tool opened, ten beam leads in the accidently strained corner opened.

c. Vibration - no additional beam leads opened. Seven of the exterior package external ribbon leads were torn from the printed circuit carrier. These were patched with new resistance welds.

d. Final Operation - The beam leads of the entire flip-flop chain remained intact through the testing, which permitted logic operation. By inserting probes through the silicone gel and pushing down on opened beam leads, various logic gate driver operations could be restored. However, the gel prevented re-connection of the opened beam leads by either silver epoxy or ultrasonics. The beam lead which was connected by silver epoxy cement remained operational.

Apparently, the pc test board has a resonance in an unsupported zone, but this external item is not a part of the scope of the investigation. It could not be determined conclusively whether a faulty interconnection or a malfunctioning chip causes the operation to stop at 80°C. The "scratchy" nature of the digital wave forms just prior to stopping, indicates an intermittent in the connections, rather than in the I.C. chips.

9.4 Final Test Vehicle Assembly and Test Results

As a result of the breadboard environmental testing, the following modifications were made in microassembly (see section 8 for details):

a. More extensive heat casing of the matrix prior to bonding. A total of 16 hours processing time at +175°C was used.

b. A better weld schedule to connect the exit layer to the beamlead matrix.

c. A nickel plated p.c. test board to obtain better resistance welding of the exit tabs.

d. A clean, loose, copper plate as a top cover to the test vehicle so that the interior could be examined more easily.

e. A sheet of "Silastic" gasket extending over the entire environmental test fixture to discourage resonances in the exterior p.c. test board.

At 4.0 volts about 82 ma drain was noted, with 80 KC clock pulse driving the fully operating flip-flop chain. Fifteen output drivers produce the correct negative pulse. Tab #39 (weld nugget #19) appeared to have an open and showed only clock pickup signal.

In the 14 hours of beam lead matrix temperature curing at +175°C the thermoplastic adhesives used in the original laminate wicked out onto the etched away areas of the laminate. The remaining adhesive was insufficient to prevent delimination of some conductors, particularly long runs of over one-half inch.

One such conductor was broken during chip bonding by snagging against the ultrasonic tool tip. This was spliced together using silver epoxy cement.

An adjusted set of ultrasonic bonding parameters was used to bond the beam leads to the 16 chips. See section 2 for details. As a result, the bonds were of more consistent appearance than in the bread board model. Nevertheless, three bond attempt out of the total 352 beam leads did not adhere. The failures appeared to be faulty aluminum lands or at least partly delaminated lands on the I.C. chips where extra needle probing had been performed. See section 6.1.10 for details of this condition.

The three beam leads which could not be ultrasonically bonded were cemented into place with minute drops of silver epoxy cement, which was then oven heated for curing and outgassing prior to gel encapsulation.

9.4.1 Temperature Test. Four cycles were run with the test vehicle operating in a chamber from +25°C up to +135°C, (+10° over the +125°C requirement). At +134°C the logic signals become irregular and at +135°C the flip-flop chain stopped operating. Cooling back down below +134°C restored normal operation. No breakage or strain in

the beam-lead matrix could be detected. The rate of temperature change was 25°C rise each 15 minutes. At 115°C the line driver signal at tab #43 (Weld nugget #21) reduced in amplitude to about 1/2 the normal 2.5V swing and the power supply current jumped from 82 to 90 ma. All other line drivers produced normal output signals over the temperature range. Output #19 remained without normal waveform.

With the same test set up the test vehicle was operated in a chamber from +25°C down to -55°C for four cycles. The flip-flop chain and the line drivers remain operating throughout this temperature cycle. Output 19 appeared restored, but output 22 showed open.

9.4.2 Impact Test. The test vehicle was given one impact test in each of its three axes. The shock was a rising sawtooth of acceleration, from 0 g to 208 g, in 3.5 milliseconds and then dropping to 0 g by 5 milliseconds. Signals were not monitored during test and the test vehicle was clamped in the environmental test fixture apparatus, ITTFL D-2309699.

9.4.3 Vibration Test. The test vehicle was vibrated through one sweep of 20 to 3000 cps on each of the three axes. The sweep rate was four octaves per minute. The acceleration was 18 g from 20 to 22 cps; then 20 g from 22 to 500 cps; then 50 g from 500 to 3000 cps. Signals were not monitored during the test and the test vehicle was clamped in the environmental test fixture apparatus.

9.4.4 Thermal Shock Test. The test vehicle was stabilized for 15 minutes at +175°C and then manually placed in a -55°C chamber within a 15 second interval of transition. Operation was then verified at room temperature. A reverse shock was performed, going from -55°C up to +175°C. Again operation was verified, but over the entire temperature range per the temperature test. Both outputs 19 and 22 indicated open following this test.

9.5 Conclusions of the Environmental Testing

Despite quality control problems in the chemofacture processing of the beam leads and the somewhat crude method of chip assembly, the beam lead matrix using original electrodeposited 1/2 ounce foil overplated with 0.3 mils of "watts" nickel appeared to perform well in the environmental tests. The encouraging results may be due in part to the shock and vibration energy absorbing effects of the silicone gel, which surrounds each beam lead and supports the entire matrix and exit layers of interconnection.

At one spot on the underside of the package cover, a minute speck of gel was detected after the vibration tests, indicating that there may be some flexing of the gel.

Nevertheless, in the termal tests, the full effects of expansion and contraction of dissimilar materials is present over a span of 1.125 inches, yet the matrix passes these severe tests. Therefore the conclusion must be that the beam lead principle for connecting directly to uncased silicon chips is a sound one and permits accommodation of environmental stresses without failure of the bonds, at least on a short term basis.

The persistent trouble with external ribbon leads and the exit layer weld nuggets around the edge of the test vehicle container may indicate excessive expansion and contraction of the 1.40 inch square package frame, which is molded from a silica-filled epoxy. Probably a package frame of suitable ceramic on metal could be substituted in any future investigtations to reduce the suspected stresses.

## 10.0 DOCUMENTATION

### 10.1 Categories of Drawings

The drawings made fall into five categories:

a. Experimental Drawings - parts made to conduct experiments which are not productive or which do not end up in the final test vehicle.

b. Environmental Fixture Drawings - parts made to permit holding and electrical connection while the test vehicle is under environmental stress testing.

c. Reference Drawings - support specifications, processing or fabrication instructions, assembly instructions, and electronic or electrical information for operating or testing the chip array.

d. Fabrication and Assembly Drawings - those drawings actually used to construct the test vehicle.

e. Illustrative or Project Drawings - those drawings which attempt to explain new technology or other project considerations.

10.1.1 Experimental Drawings. The following ITTFL drawings in this category have been made, but were discarded or not incorporated in the final conclusion of the studies.

D2309609, Surface Cutting Artwork, 5 Mil

A2309575, Beam Lead Artwork Pattern SE 155

B2309582, Beam Lead Pattern, SE 155

C2309583, Window Pattern, SE 155

A2309447, Specification, Double Clad 0.5 MIL Al. Laminate

C2309481, Chip Array, Flip Flop Artwork

D2309546, NASA Continuity Test Pattern

C2309569, Package Model, Uncased Chips

D2309600, Package, Module

D2309619, Bonding Test Artwork

A2309620, Bonding Test Assembly

F2309641, Eyelet Test Pattern for Plating

A2309512, Silicon Chip, Signetics Type SE 180

D2309585, Window Pattern Artwork for SE 155

10.1.2 Environmental Fixture Drawings. The following ITTFL drawings for electrical test and environmental evaluation were made:

F2309621-9 Master Artwork, P.C. Test Board

D2309699, Layout, NASA Package Mounting Frame

C2309700, Plate, Base

B2309701, Plate, Spacer

B2309702, Plate, Top

B2309703, Plate, Top

B2309704, Support, Connector

B2309705, Plate, Mounting

10.1.3 Reference Drawings. The following ITTFL reference drawings have been concerned with technology, procedure, assembly, and test of the final test vehicle:

D2309446, Typical Specification, Uncased Silicon Chip

D2309630, Positioning Diagram, Chip SE 106-C

D2309631, Positioning Diagram, Chip SE 116-C

D2309632, Positioning Diagram, Chip SE 124-C

D2309633, Positioning Diagram, Chip SE 155-C

D2309634, Positioning Diagram, Chip SE 156-C

D2309635, Positioning Diagram, Chip CS 730-C

D2309636, Positioning Diagram, Chip CS 732-C

D2309494, Logic Diagram, NASA I.C. Matrix

A2309618, Test Plan, NASA Test Vehicle

D2309669, Top Drawing Index, NASA Test Vehicle

A2309498, Probe - Ultrasonic Bonder

C2309484, Ultrasonic Bonder Tip

A2309666, Clamping Plate, Assembly Fixture

A2309649, Artwork, NASA Assembly Fixture

A2309667, Base Plate, Clamp Fixture

B2309616, Chip Holder for Ultrasonic Bonder

B2309617, Window Pattern Layout for Chip Holder

C2309615, Work Surface for Ultrasonic Bonder

10.1.4 Fabrication and Assembly Drawings. The following drawings necessary to make a test vehicle as depicted in the drawing index D2309669 were completed:

B2309658, Test Vehicle Chip Array, Customer Use

F2309657, Detailed Assembly, Chip Array

B2309664, Substrate, Ceramic

B2309665, Frame, Molded Epoxy

A2309512G1, Silicon Chip, Signetics Type SE 124C

A2309514G1, Silicon Chip, Signetics Type CS 730C

A2309514G2, Silicon Chip, Signetics Type SE 116C
A2309515G1, Silicon Chip, Signetics Type SE 155C
A2309515G2, Silicon Chip, Signetics Type SE 156C
A2309516G1, Silicon Chip, Signetics Type CS 732C
A2309516G2, Silicon Chip, Signetics Type SE 106E
B2309661G1, Spacer, Bottom Insulator
F2309621, Artwork, Spacer Cutting Pattern
B2309662, Exit Matrix Layer
F2309599, Layout, Exit Nugget Pattern
F2309621-6, Artwork; Exit Layer Cutting Holes
F2309621-8, Artwork; Surface Conductors
F2309631-11, Artwork; Jig and Blanking
F2309621-7, Artwork; Nugget Plating
F2309621-10, Artwork; Ribbon Lead Build-Up
B2309660, Wiring Beam-Lead Matrix, Two Layer
F2309642, Matrix Surface - Pattern Layout
D2309589, Finger Pattern for CS 730C
D2309590, Finger Pattern for SE 116C
D2309591, Finger Pattern for CS 732C
D2309592, Finger Pattern for SE 106C
D2309593, Finger Pattern for SE 156C
D2309594, Finger Pattern for SE 155C
D2309595, Finger Pattern for SE 124C
F2309621-1, Artwork; Matrix Cutting Holes
F2309621-2, Artwork; Nugget Plating, Matrix
F2309621-3, Artwork; Conductor Surface No. 1
F2309621-4, Artwork; Conductor Surface No. 2
F2309621-5, Artwork; Window, Jig, and Blanking

10.1.5 Illustrative and Project Drawings. The following ITTFL drawings in this category were made:

C2309740, Study Plan (Time), NASA Contract
A2309602, Corner of a Typical Chip Array (Figure 1)
A2309603, Cross Section of a Beam Lead and Matrix (Figure 2)
A2309604, Cross Section Through a Packaged Assembly (Figure 3)

A2309605, Close Up View of a Finger Pattern and Beam Leads (Figure 4)

A2309606, Matrix Dimensional Standards (Figure 5)

A2309607, Typical Subsystem Package Dimensions (Figure 6)

10.2.1 Complexity Level of Engineering Drawings. The documentation required to engineer a large-scale chip array using a variety of non-standard chip sizes and non-standard aluminized exit lands is comparable in scope and elapsed time to that of a custom complex function silicon integrated function, but considerably less complex than the engineering for a Large Scale Integration (LSI) integrated on a silicon master slice.

Considerable engineering economy could be achieved with the use of a standard chip size and a standard pattern of land locations around the periphery of the chip types, regardless of the circuit element patterns diffused into the silicon surface.

## 11.0 RECOMMENDATIONS FOR FURTHER INVESTIGATION

### 11.1 Summary of Goals

The achievements and problems encountered in the course of this study lead to the following suggestions of areas worthy of additional study and of specific tasks for implementing this work.

a. Improve the technical performance in the areas of difficulty described in the program summary.

b. Increase the flexibility of application by including passive thick film circuit elements and special-parameter discrete chips into the overall structural organization. Interface connections between the beam-lead matrix, the thick film circuit elements, and the discrete chip "add-ons" must all be compatible.

c. Provide small alterations to the design features of the hybrid microassembly which assure that the construction is adaptable to automated microassembly.

### 11.2 Detailed Kapton Investigation

a. Demonstrate the level of dielectric etching resolution obtainable with Kapton laminates from at least two vendors.

b. Using typical matrix surface patterns ordinarily used with chip arrays, determine the curve of Kapton shrinkage vs. oven curing temperatures for temperatures up through 175 degree centigrade.

c. Assemble three test sections of Kapton chip arrary each containing 46 silicon diodes on eight or more different chips. Perform sustained, elevated temperature, back-bias leakage tests within sealed containers for the following three variations in assembly:

   a. Vacuum bakeout, inert gas

   b. Vacuum bakeout, silicone coating

   c. Vacuum bakeout, silicone gel encapsulant.

Establish the "high-reliability" adequacy of Kapton as an organic dielectric within a sealed enclosure, in the light of data indicating that is tends to absorb moisture, by comparison of the changes in back-bias leakage measured above to values for the same type of chip sealed conventionally in ceramic flatpacks.

### 11.3 Matrix to Substrate Connections

Establish a fixed connection method between the beam lead matrix and thick film terminals on an alumina substrate. If the Kapton is chemically "blanked" to face a tab shaped structure which is hinged to the matrix at one end, it should be possible to bend it downward to the alumina substrate surface.

The following features must be determined:

a. Should the tab contain a Kapton core?

b. What plated metals provide high bond strength to which types of thick film surface?

c. Will the use of soldering provide an adequate thermal performance or will ultrasonic bonding be required?

d. How small can the width and length of the tab be made (to conserve matrix area) and remain trustworthy in the stressed environmental conditions?

e. Are there long-term corrosion or metal-to-metal compounds which could threaten the future performance of the bond?

## 11.4 Matrix to Discrete and I.C. Chips

Establish a beam-lead connection method, between the beam lead matrix and the I.C. chips which uses selected metal platings to the outer surface of each beam lead. The following features must be determined:

a. Can the uniformity of plating adhesion strength of the added metal be demonstrated as determined by consistent bonding performance and environmental stress testing?

b. What rules can be established as the appropriate metal or sequence of metals to be plated according to the metallurgy of the chip terminals, i.e. capacitor monoblocks, special transistor terminals, as well as the more typical aluminum pads and solder bumps?

c. When should hybrid add on chips be more reliably electrically connected to the thick film substrate directly (such a flip-chip bonding, jumper leads, etc.) as opposed to the alternative of tying in with the overhead matrix?

## 11.5 Beam Lead Attachment Process

Determine the relative merits between simultaneous bonding of an entire finger pattern of beam leads and the bonding of individual beam leads one by one in a sequential manner. The following features must be determined:

a. Can the I.C. "flip-chip" positioning mechanisms now available be used to attach I.C. chips having 14 or more terminal pads into a beam lead matrix?

b. Can the chips be bonded into the matrix prior to attachment of the bases of the chips to the thick film substrate?

c. Can a difference in the quality and stressed environmental performance be detected between single beam lead bonds and simultaneous multiple bonds?

## 11.6 Hybrid Study Vehicle

A suitable series of partial or complete assemblies using the same hybrid function must be built to demonstrate or determine the results to the questions presented in the previous tasks. This function must preferably contain a cluster of digital I.C. chips, several analog I.C. chips, several special-purpose discrete transistor silicon chips, at least one high-capacitance add-on capacitive by-pass chip, and a number of one-percent thick film resistors integral to an aluminum substrate.

In order to reduce extraneous packaging considerations, the hybrid function should not involve more than 20 to 24 add-on chips nor should it involve more than 40 external-world connections so that a commercially available hermetic container can be used.